RSU7N65F

VDSS

650V

Lead Free Package and Finish

Super Junction MOSFETs

Applications:

- •Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- •PFC stages for server & telecom
- •Consumer

Features:

- •New revolutionary high voltage technology
- •Better RDS(on) in TO-220F
- •Ultra Low Gate Charge cause lower driving requirements
- ·Periodic avalanche rated
- •Ultra low effective capacitances

G_{DS} 1.Gate o 3.Source

RDS(ON)(Max.)

650mΩ

Ordering Information

Part Number	Package	Marki ng
RSU7N65F	TO-220F	RSU7N65F

Absolute Maximun Ratings $Tc=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	RSU7N65F	Units	
VDSS	Drain-to-Source Voltage	650	V	
ID	Continuous Drain Current (TC = 25℃)	7		
ID	Continuous Drain Current (TC = 100℃)	4	Α	
Ірм	Pulsed Drain Current (Note*1)	21	1	
PD	Power Dissipation(Tc=25℃)	32	W	
VGS	Gate-to-Source Voltage	±30	V	
EAS	Single Pulse Avalanche Engergy (Note*2)	120	mJ	
IAR	Avalanche Current pulse width limited by maximum junction temperature.	1.2	А	
	Maximum Temperature for Soldering			
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	300 260	$^{\circ}\mathrm{C}$	
	Package Body for 10 seconds			
TJ and TSTG	Operating Junction and Storage	-55 to 150		
To allu ToTG	Temperature Range	-33 (0 130		

ID **7A**

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSU7N65F	Units	Test Conditions
RθJC	Junction-to-Case	4	.c\m	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	68]	1 cubic foot chamber,free air.

^{*}Drain Current Limited by Maximum Junction Temperature



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OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650	1	1	V	VGS = 0V, ID = 250 μ A, TJ= 25 $^{\circ}$ C
			650	1	٧	VGS = 0V, ID = 250 μ A, TJ= 150 $^{\circ}$ C
IDSS	Drain-to-Source Leakage Current			1.0	μΑ	VDS=650V,VGS=0V
IGSS	Gate-to-Source Forward Leakage		-	100	_	VGS=+30V VDS=0V
	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		560	650	mΩ	VGS=10V,ID=3.5A
VGS(TH)	Gate Threshold Voltage	2.5		4.0	V	VGS=VDS,ID=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		11.6		- - ns	VDS=400V ID=3.5A RG=25Ω VGS=10V
trise	Rise Time		23			
td(OFF)	Turn-OFF Delay Time		53			
tfall	Fall Time		35.8			

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		493		pF	VGS=0V VDS=100V f=1.0MHz VDS=520V ID=3.5A VGS=10V
Coss	Output Capacitance		32			
Crss	Reverse Transfer Capacitance		1.6			
Qg	Total Gate Charge		2.8		nC	
Qgs	Gate-to-Source Charge		4.7			
Qgd	Gate-to-Drain("Miller") Charge		13.3			

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Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current		-	7	Α	Integral pn-diode
ISM	Maximum Pulsed Current		-	21	Α	in MOSFET
VSD	Diode Forward Voltage		0.85		V	IS=3.5A,VGS=0V Tj=25℃
trr	Reverse Recovery Time		201		nS	VD-50V/V00-0V
Qrr	Reverse Recovery Charge		1.3		μC	VR=50V,VGS=0V IS=3.5A,di/dt=100A/
Irrm	Peak Reverse Recovery Current		11.5		Α	µs

Notes:

El ectri cal Characteri sti csDi agrams

Figure 1. Output Characteristics

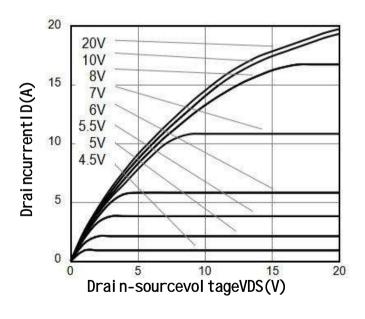
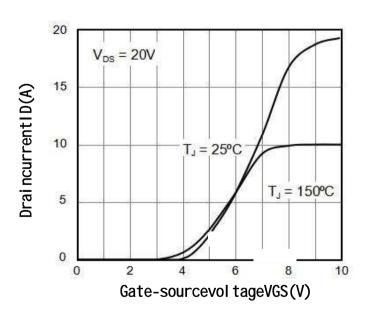


Figure 2. Transfer Characteristics



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^{*1.}Repetitive rating; pulse width limited by maximum junction temperature.

^{*2.} Pulse width tp limited by Tj,max

Figure 3. On-Resistancevs. DrainCurrent

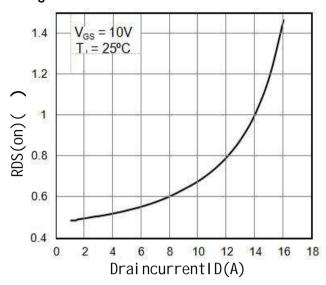


Figure5. GateChargeCharacteristics

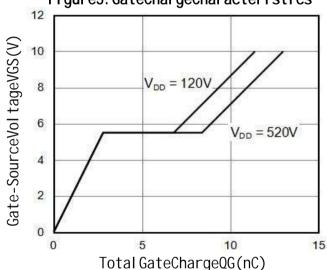


Figure 7. Breakdown Voltagevs. Temperature

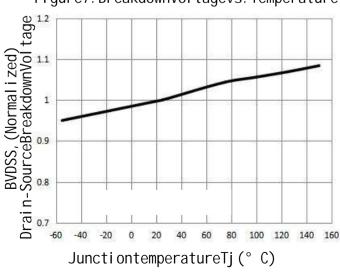
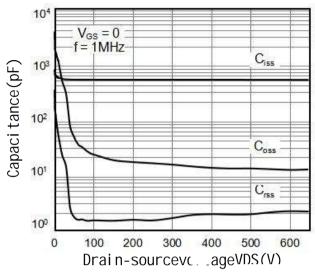


Figure 4. Capacitance Characteristics



Fi gure6. BodyDi odeForwardVol tage

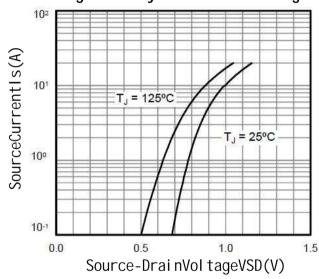
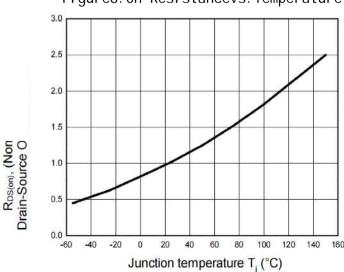
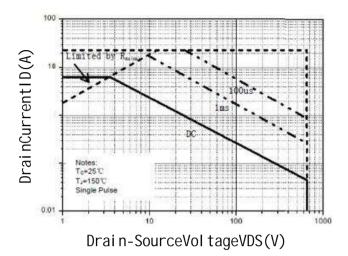


Figure 8. On-Resistance vs. Temperature



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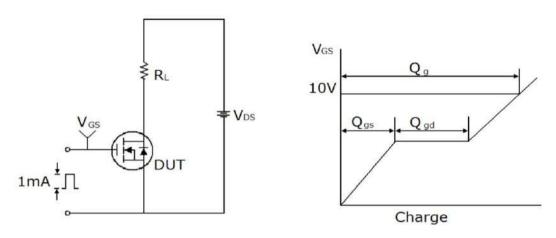
Figure 9. Maxi mumSafe Operating Area



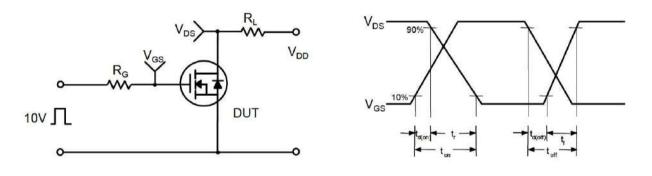


Test Circuits and Waveforms

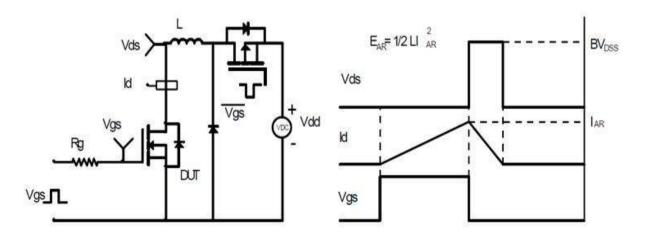
GateChargeTestCircuit&Waveform



SwitchingTestCircuit&Waveform



UnclampedInductiveSwitchingTestCircuit&Waveform



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