

Multi-Epi Super Junction MOSFETs



Lead Free Package and Finish

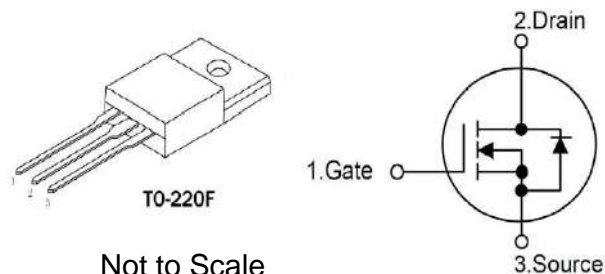
Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- PFC stages for server & telecom
- Consumer

ID	RDS(ON)(Max.)	VDSS
13A	380mΩ	650V

Features:

- New revolutionary high voltage technology
- Better RDS(on) in TO-220F
- Ultra Low Gate Charge cause lower driving requirements
- Periodic avalanche rated
- Ultra low effective capacitances



Ordering Information

Part Number	Package	Marking
RSU13N65F	TO-220F	RSU13N65F

Absolute Maximum Ratings $T_c=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	RSU13N65F	Units
VDSS	Drain-to-Source Voltage (Note*1)	650	V
ID	Continuous Drain Current	13	A
IDM	Pulsed Drain Current (Note*2)	46	
PD	Power Dissipation($T_c=25^{\circ}\text{C}$)	33	W
VGS	Gate-to-Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy $L=60\text{mH}$, $I_{AS}=3\text{A}$, $V_{DD}=150\text{V}$, Starting $T_J=25^{\circ}\text{C}$	280	mJ
IAR	Avalanche Current	2.3	A
EAR	Repetitive Avalanche Energy	1.2	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	$^{\circ}\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds		
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RSU13N65F	Units	Test Conditions
RθJC	Junction-to-Case	3.78	$^{\circ}\text{C}/\text{W}$	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of $+150^{\circ}\text{C}$.
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.

OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650	--	--	V	VGS = 0V, ID = 250μA, TJ= 25°C
		--	700	--	V	VGS = 0V, ID = 250μA, TJ= 150°C
IDSS	Drain-to-Source Leakage Current	--	--	1.0	μA	VDS=650V, VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+30V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (NOTE*3)	--	340	380	mΩ	VGS=10V, ID=6.5A
VGS(TH)	Gate Threshold Voltage	2.5	--	4.5	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	17	--	ns	VDS=400V ID=6.5A RG=20Ω VGS=10V
trise	Rise Time	--	12	--		
td(OFF)	Turn-OFF Delay Time	--	130	--		
tfall	Fall Time	--	10	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	780	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	23	--		
Crss	Reverse Transfer Capacitance	--	1.9	--		
Qg	Total Gate Charge	--	34	--	nC	VDS=400V ID=6.5A VGS=10V
Qgs	Gate-to-Source Charge	--	4.5	--		
Qgd	Gate-to-Drain("Miller") Charge	--	19	--		

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RSU13N65F

Source-Drain Diode Characteristics

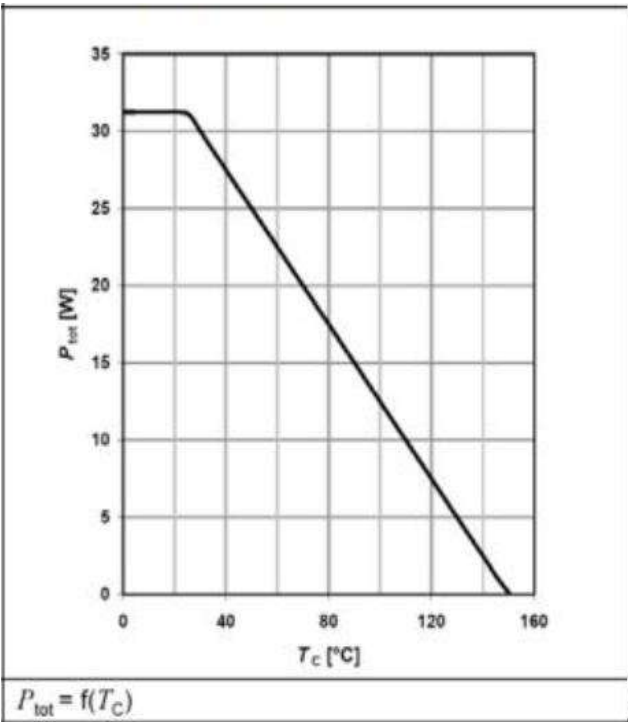
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	10.0	A	Integral pn-diode in MOSFET
ISM	Maximum Pulsed Current	--	--	35	A	
VSD	Diode Forward Voltage	--	0.9	1.5	V	IS=6.5A,VGS=0V Tj=25℃
trr	Reverse Recovery Time	--	300	--	nS	VGS=0V IS=6.5A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	3.5	--	μC	

Notes:

- *1.TJ=±25℃ to +150℃.
- *2.Repetitive rating;pulse width limited by maximum junction temperature.
- *3.. Pulse Test: Pulse width ≤ 300us, Duty Cycle ≤2%

Typical Feature curve Tj=25℃, unless otherwise noted

Fingure1. Power dissipation



Fingure2. Max. transient thermal impedance

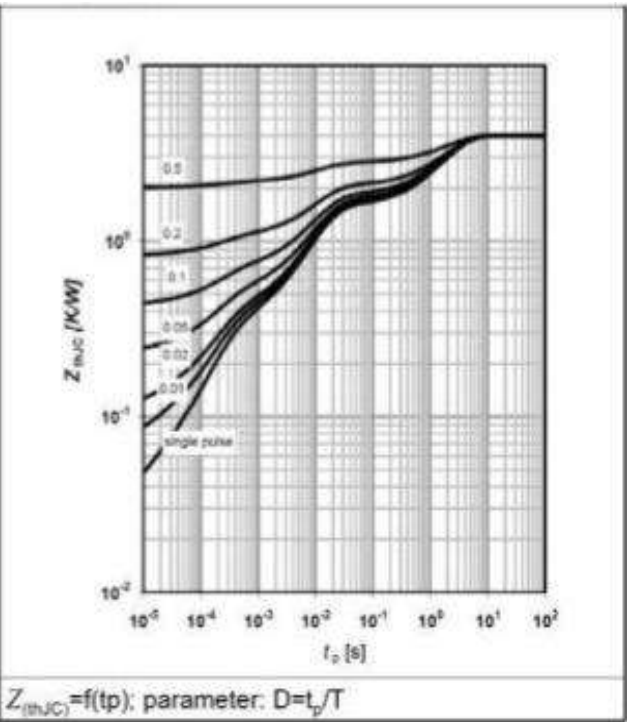


Figure3. Safe operating area $T_c=25^\circ\text{C}$

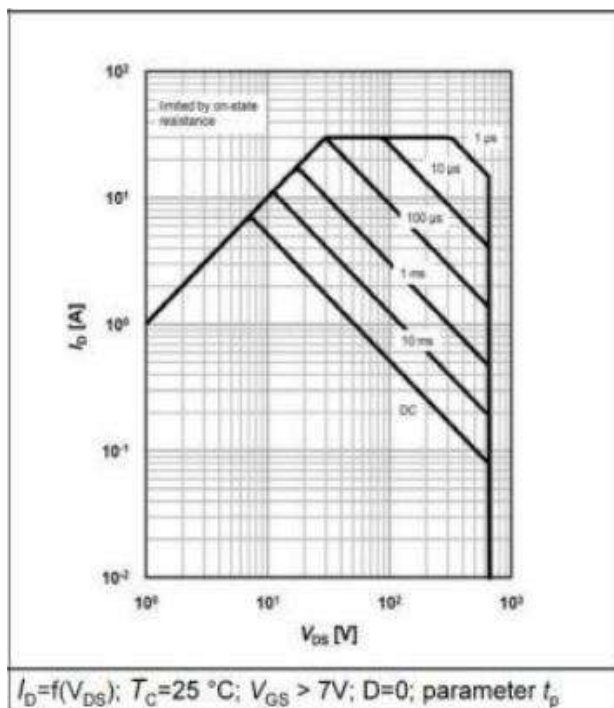


Figure4. Safe operating area $T_c=80^\circ\text{C}$

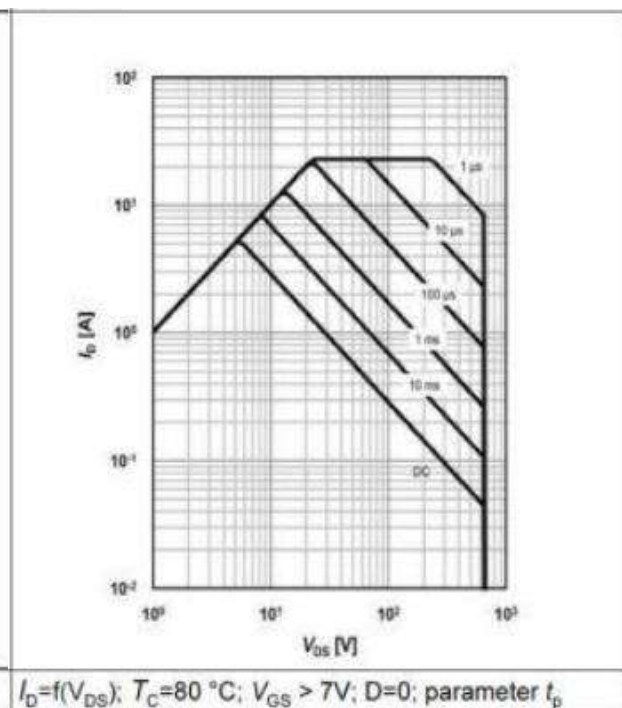


Figure5. Output characteristics $T_j=25^\circ\text{C}$

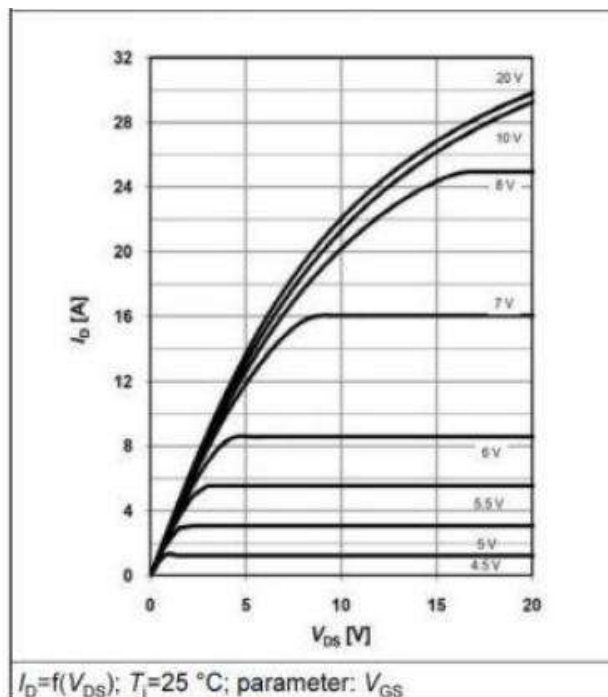


Figure6. Output characteristics $T_j=125^\circ\text{C}$

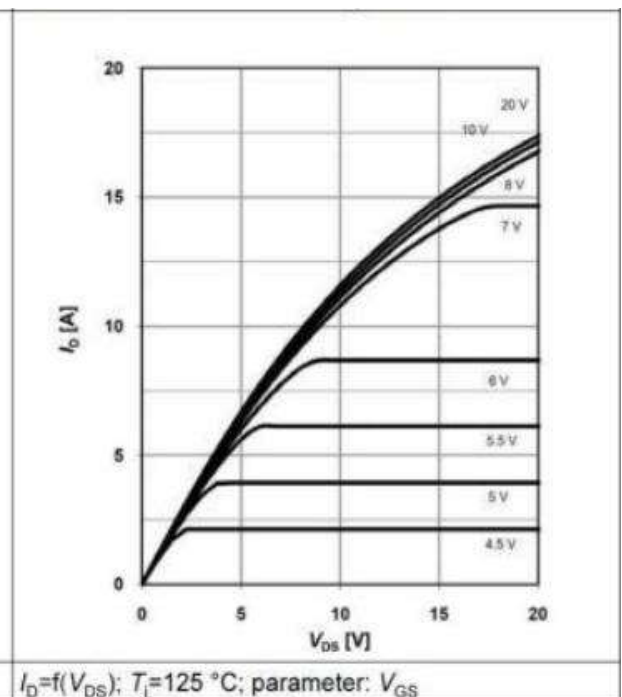


Figure7. Type drain-source on state resistance

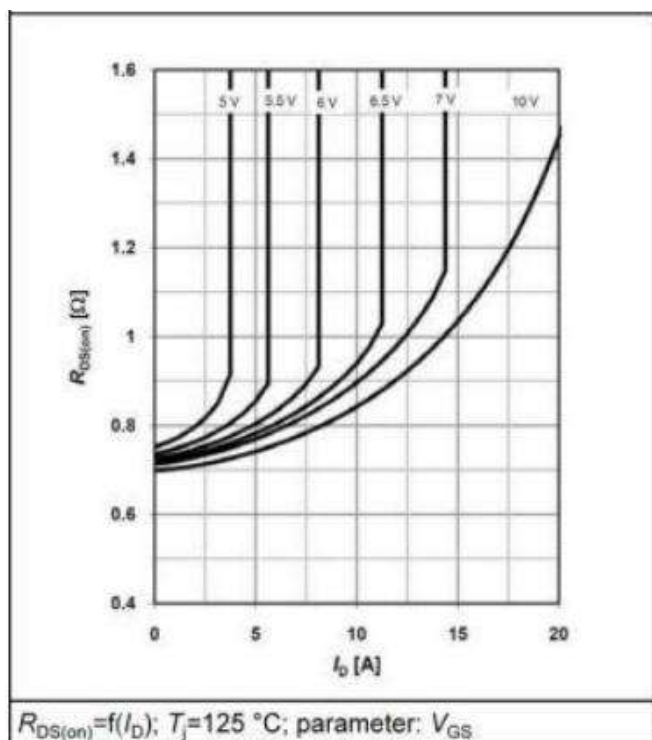


Figure8. Typ. drain-source on state resistance

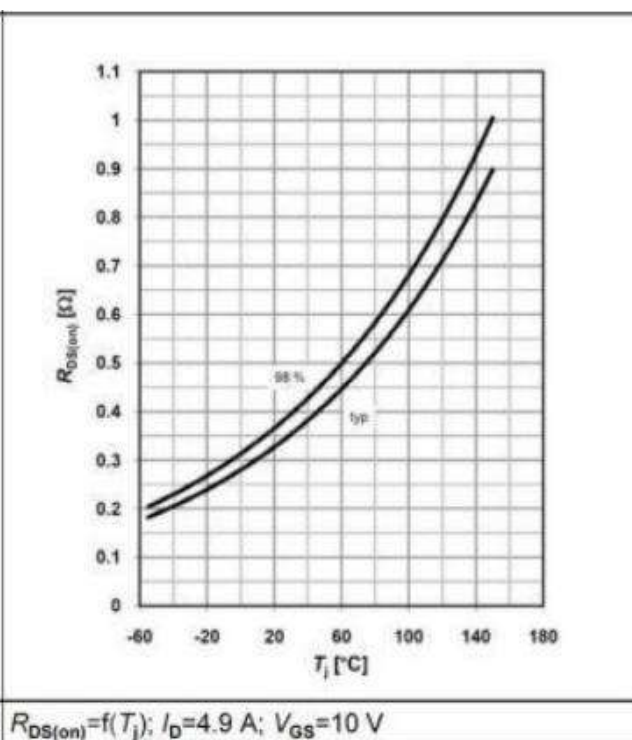


Figure9. Typ. transfer characteristics

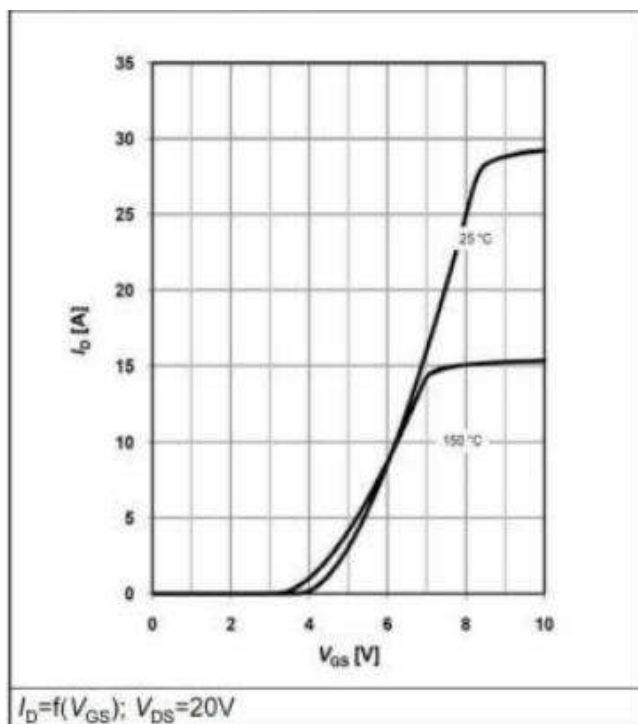


Figure10. Gate charge

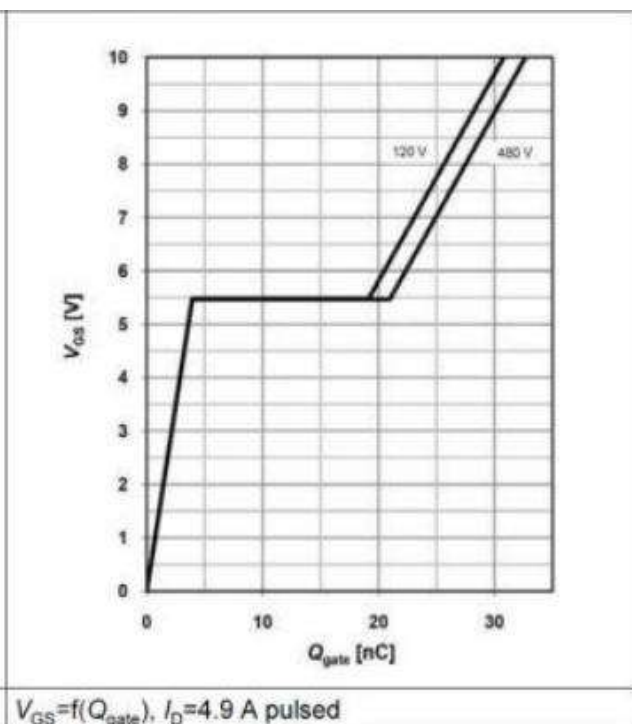


Figure11. Avalanche energy

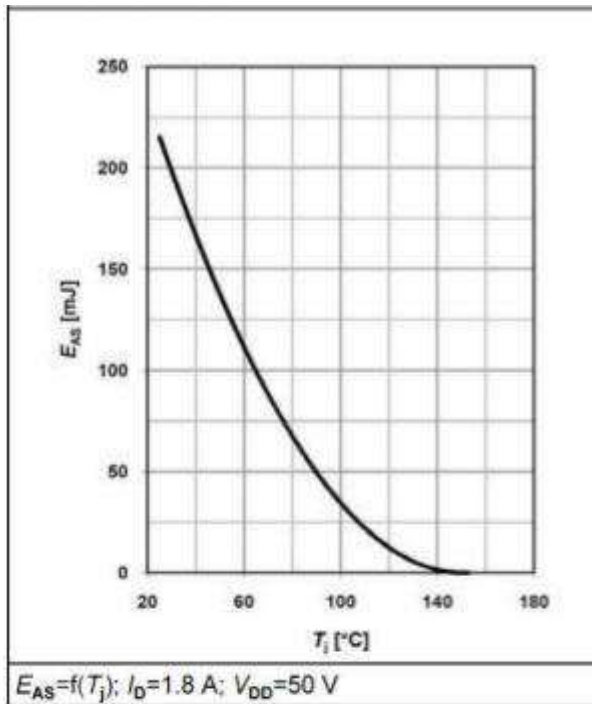


Figure12. Drain-source breakdown voltage

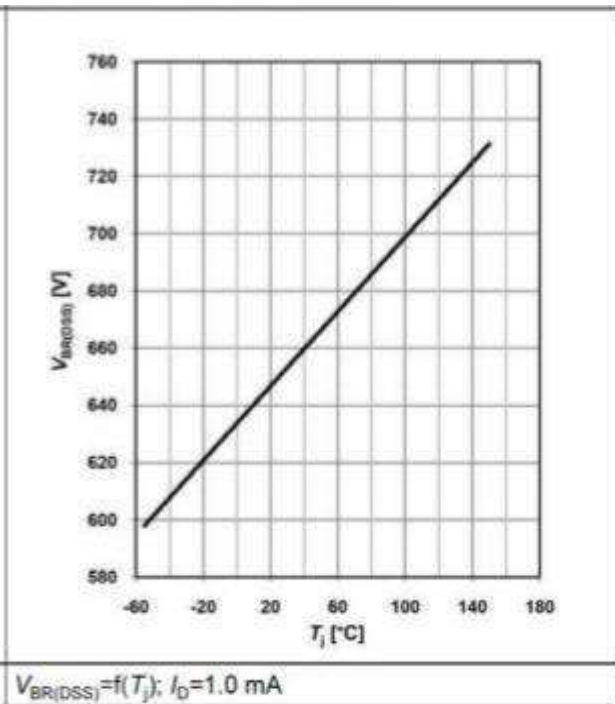


Figure13. Typ. capacitances

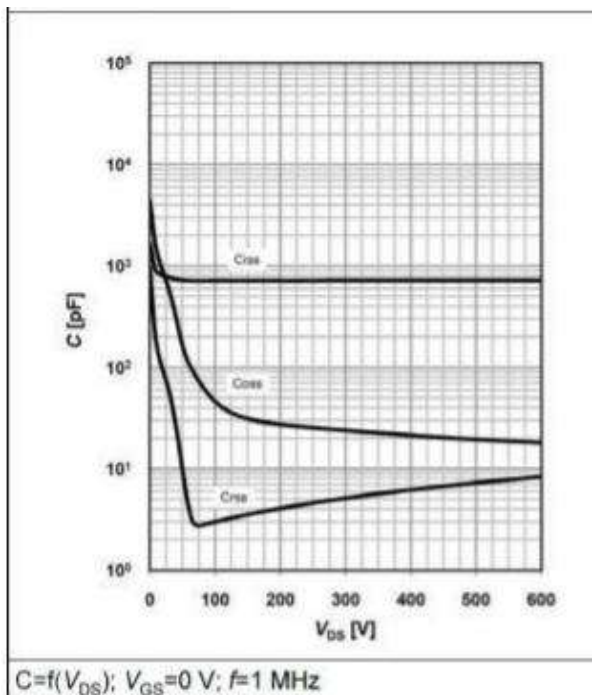
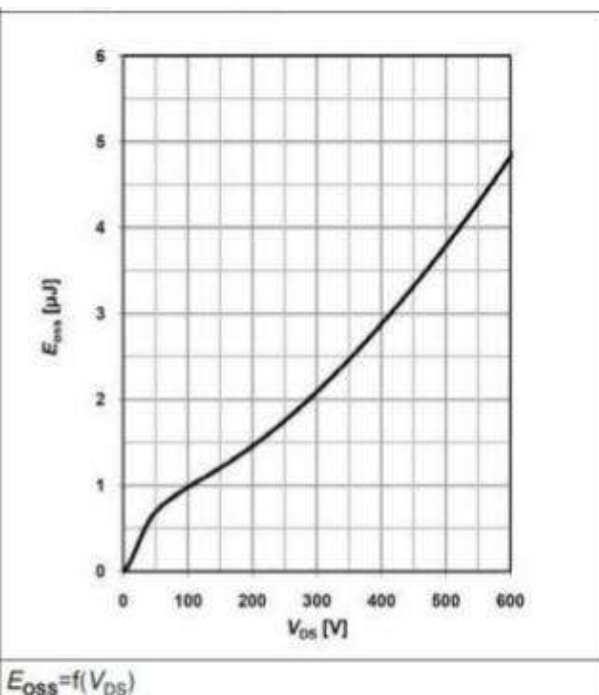


Figure14. Coss stored energy



Test Circuits and Waveforms

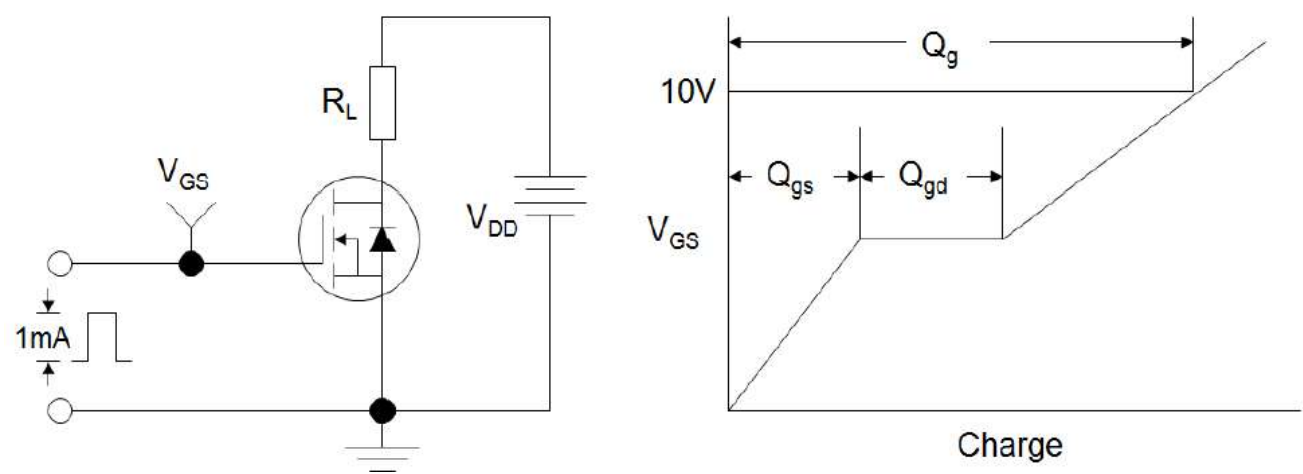


Figure A.
Gate Charge Test Circuit and Waveform

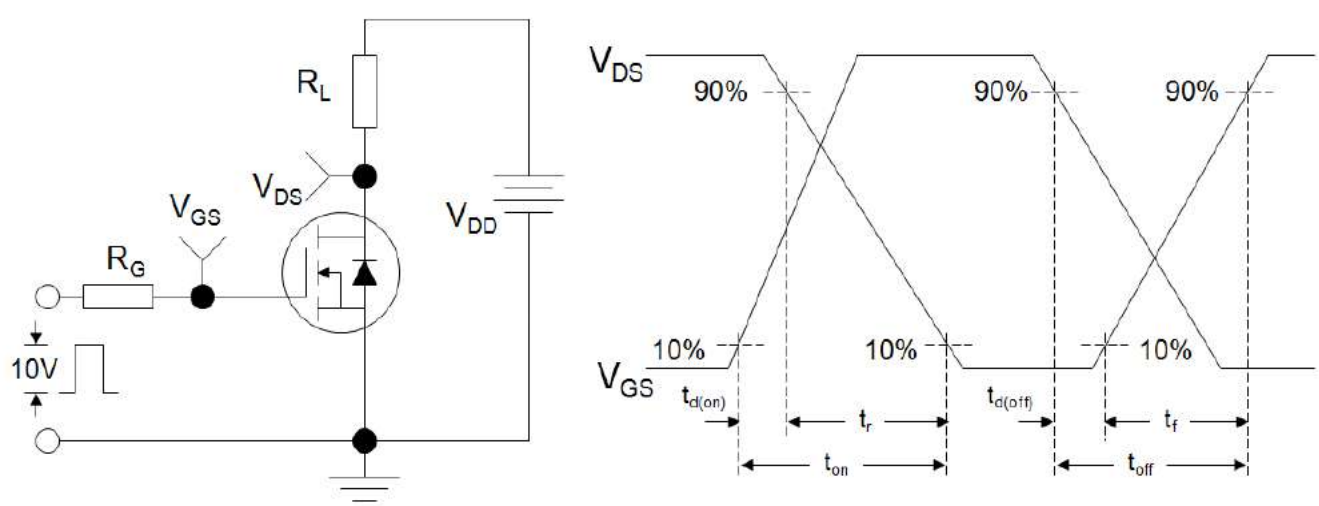


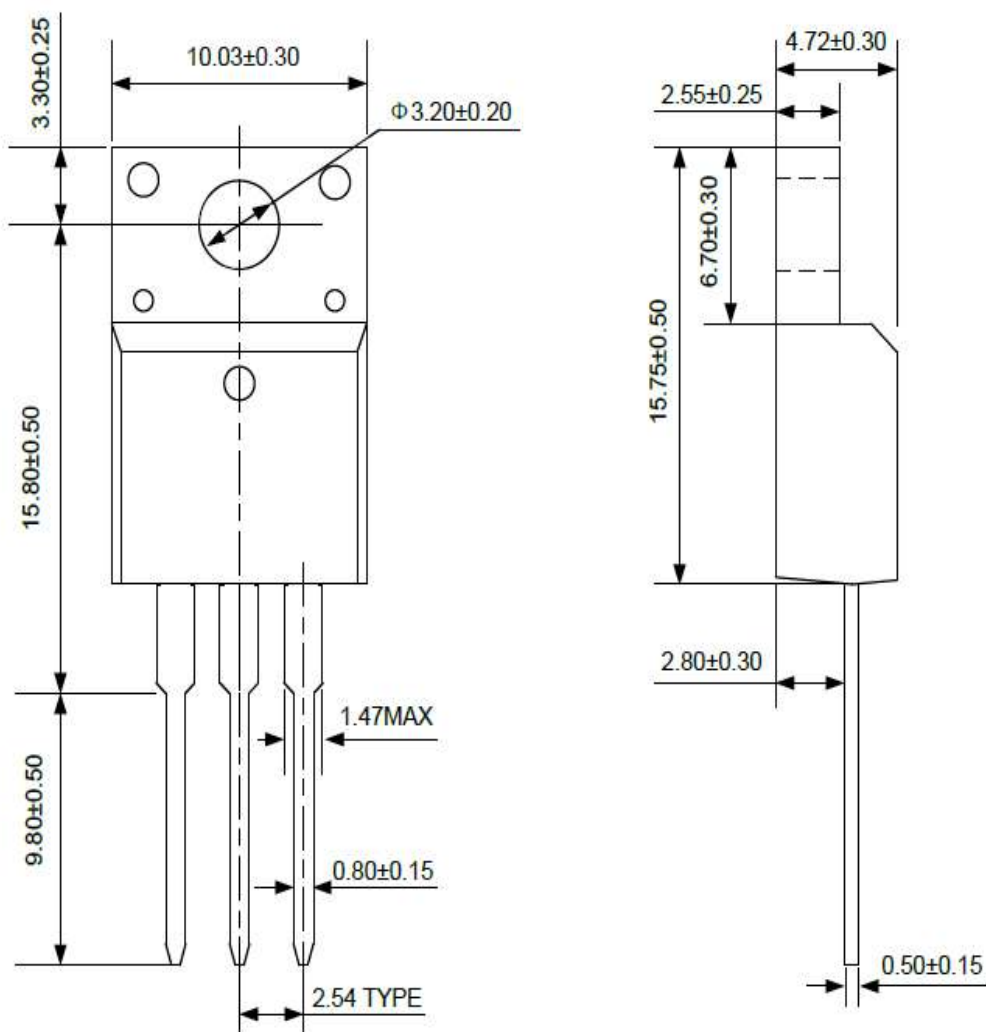
Figure B.
Resistive Switching Test Circuit and Waveform

Test Circuits and Waveforms

Figure C.Unclamped Inductive Switching Test Circuit and Waveform

Package outline drawing

Unit:mm



TO-220F

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