### RSU11N65F

**V**DSS

650V

#### **Multi-Epi Super Junction MOSFETs**

# P6)

ΙD

11A

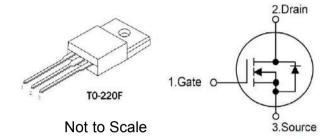
Lead Free Package and Finish

### Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- •PFC stages for server & telecom
- •Consumer

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- New revolutionary high voltage technology
- •Better RDS(on) in TO-220F
- •Ultra Low Gate Charge cause lower driving requirements
- •Periodic avalanche rated
- •Ultra low effective capacitances



RDS(ON)(Max.)

420mΩ

### **Ordering Information**

Part Number	Package	Marking
RSU11N65F	TO-220F	RSU11N65F

### Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RSU11N65F	Units
VDSS	Drain-to-Source Voltage (Note*1)	650	V
ID	Continuous Drain Current	11	^
IDМ	Pulsed Drain Current (Note*2)	42	A
PD	Power Dissipation(Tc=25℃)	32.5	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=60mH, IAS=3A, VDD=150V, Starting TJ=25 ℃	260	mJ
IAR	Avalanche Current	2.0	Α
EAR	Repetitive Avalanche Engergy	1	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	$^{\circ}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

<sup>\*</sup>Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

#### **Thermal Resistance**

Symbol	Parameter	RSU11N65F	Units	Test Conditions
RθJC	Junction-to-Case	3.85	.C\M	Drain lead soldered to water cooled heatsink,PD  Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.



## RSU11N65F

### OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
DV/DSS	Drain to source Preakdown Voltage	650	-		I \/	VGS = 0V, ID = 250 $\mu$ A, TJ= 25 $^{\circ}$ C
BVDSS	Drain-to-source Breakdown Voltage		700		I \/	VGS = 0V, ID = 250µA, TJ= 150℃
IDSS	Drain-to-Source Leakage Current			1.0	μA	VDS=650V,VGS=0V
IGSS	Gate-to-Source Forward Leakage			100		VGS=+30V VDS=0V
1633	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

### ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (NOTE*3)	-	380	420	mΩ	VGS=10V,ID=5.5A
VGS(TH)	Gate Threshold Voltage	2.5		4.5	V	VGS=VDS,ID=250μA

### Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		15			VDS=400V
trise	Rise Time		10		20	ID=5.5A
td(OFF)	Turn-OFF Delay Time		110		ns	RG=20Ω
tfall	Fall Time		9			VGS=10V

### **Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		720			VGS=0V
Coss	Output Capacitance		20		pF	VDS=25V
Crss	Reverse Transfer Capacitance		1.5			f=1.0MHz
Qg	Total Gate Charge		32			VDS=400V
Qgs	Gate-to-Source Charge		4		nC	ID=5.5A
Qgd	Gate-to-Drain("Miller") Charge		16			VGS=10V

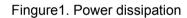
## RSU11N65F

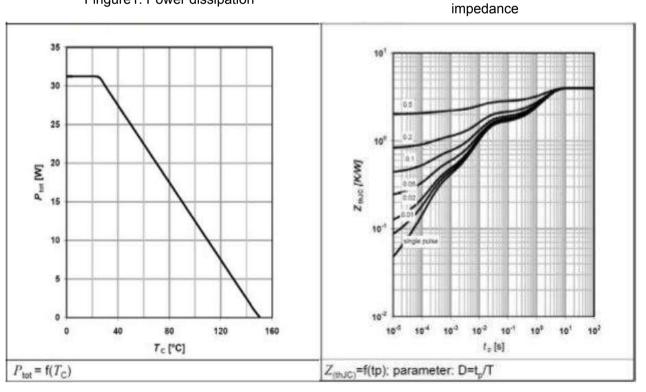
#### **Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	<b>Test Conditions</b>
IS	Continuous Source Current		-	9.2	Α	Integral pn-diode
ISM	Maximum Pulsed Current		-	30	Α	in MOSFET
VSD	Diode Forward Voltage		0.9	1.5	V	IS=5.5A,VGS=0V Tj=25℃
trr	Reverse Recovery Time		280		nS	VGS=0V
Qrr	Reverse Recovery Charge		3.3		μC	IS=5.5A,di/dt=100A/µs

#### Notes:

### Typical Feature curve $T_J=25^{\circ}C$ , unless otherwise noted





Fingure2. Max. transient thermal

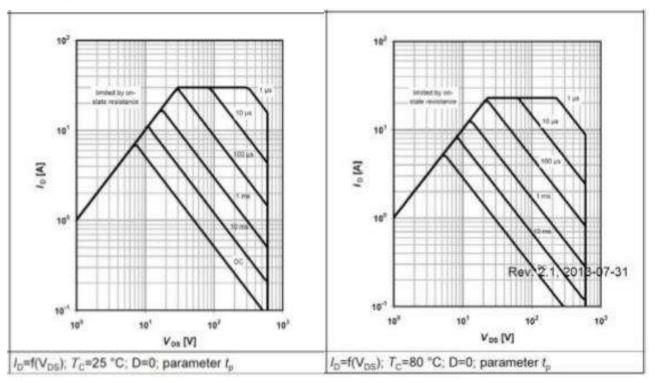
<sup>\*1.</sup>TJ=±25℃ to +150℃.

<sup>\*2.</sup>Repetitive rating; pulse width limited by maximum junction temperature.

<sup>\*3..</sup> Pulse Test: Pulse width  $\leq$  300us, Duty Cycle  $\leq$  2%

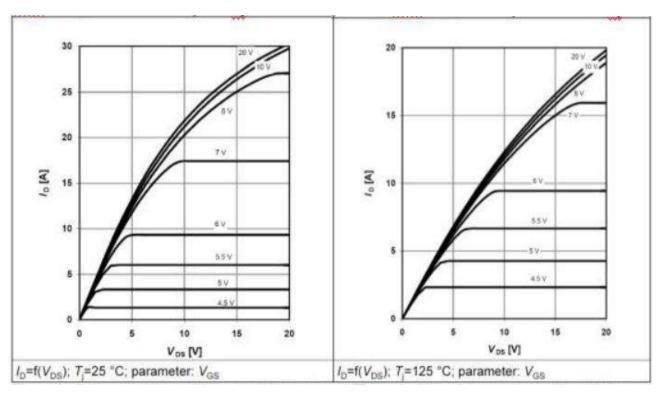
Fingure3. Safe operating areaTc=25℃

Fingure4. Safe operating areaTc=80°C



Fingure5. Output characteristics Tj=25℃

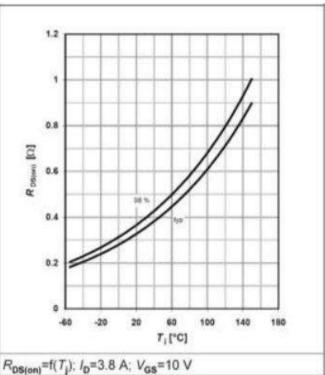
Fingure6. Output characteristics Tj=125°C



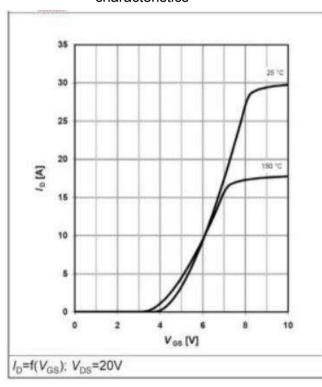
## RSU11N65F

Fingure7. Type drain-source on state resistance

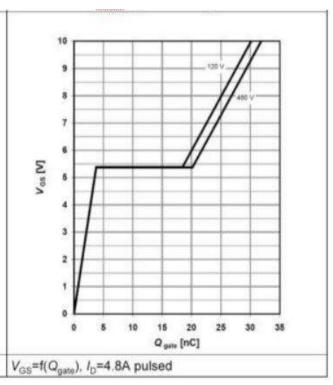
Fingure8. Typ. drain-source on state resistance



Fingure9. Typ. transfer characteristics

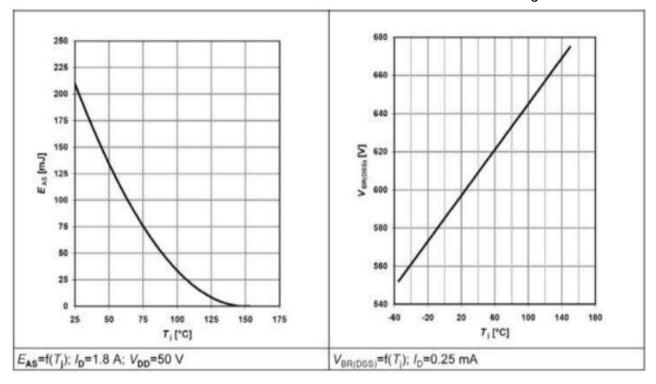


Fingure 10. Gate charge



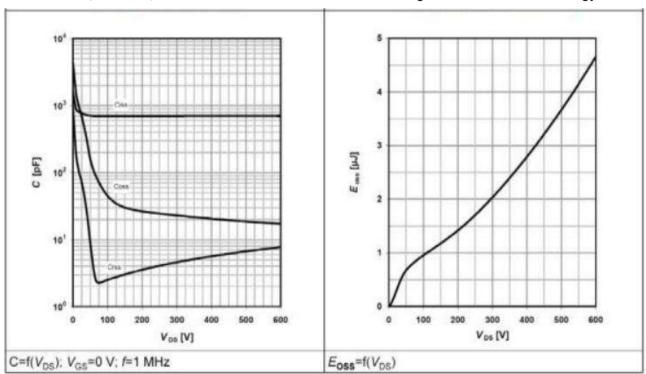
Fingure 11. Avalanche energy

Fingure 12. Drain-source breakdown voltage



Fingure 13. Typ. capacitances

Fingure14. Coss stored energy



### **Test Circuits and Waveforms**

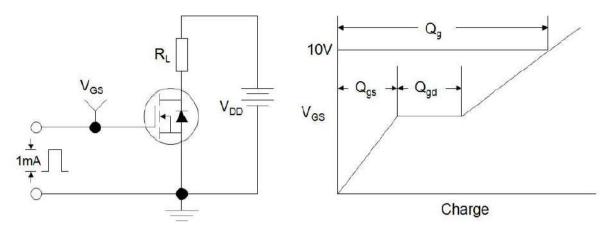


Figure A.
Gate Charge Test Circuit and Waveform

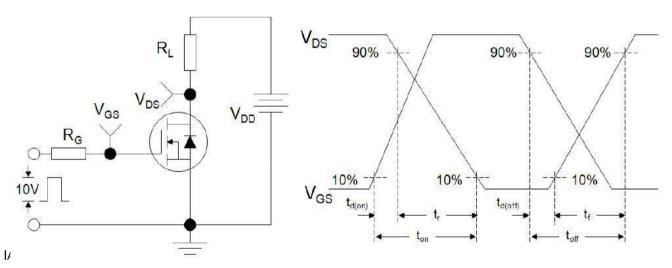


Figure B.
Resistive Switching Test Circuit and Waveform

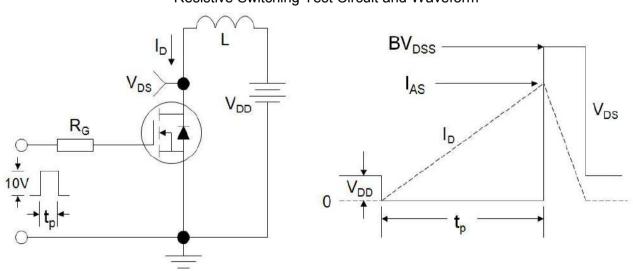
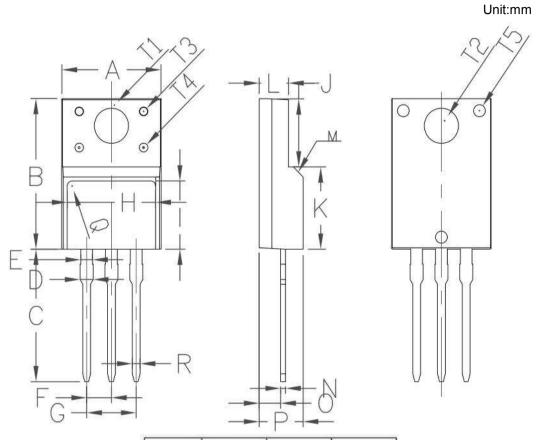


Figure C.Unclamped Inductive Switching Test Circuit and Waveform Copyright Reasunos http://www.reasunos.com REV:A0 Feb.2019



# Package outline drawing



Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
С	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
Н	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8. 99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
0	2.15	2.35	2,55
P	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3.45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83

### RSU11N65F

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