REASUNOS

RS9N65D

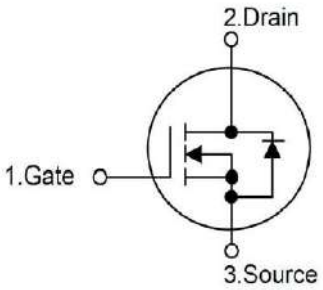
N Channel MOSFET

Lead Free Package and Finish

Applications:

- •Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
9A	0.9Ω	650V



Features:

- •Fast switching
- •100% avalanche tested
- •Improved dv/dt capability
- •RoHS Compliant

Ordering Information

Part Number	Package	Marking
RS9N65D	TO-252	RS9N65D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS9N65D	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	650	V
I_D	Continuous Drain Current	9	A
I_{DM}	Pulsed Drain Current (Note*2)	36	
P_D	Power Dissipation	70	W
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Engergy L=10mH V_{DD}=50V R_G=25Ω T_J=25℃	210	mJ
T_L	Maximum Temperature for Soldering	300	℃
T_{PKG}	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS9N65D	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.78	℃/W	Drain lead soldered to water cooled heatsink,P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	60		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	650	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=650V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance (Note*3)	--	0.9	1.08	Ω	V_{GS}=10V,I_D=4.5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	23	--	nS	V_{DS}=325V I_D=9A R_G=25Ω (Note:3,4)
t_{rise}	Rise Time	--	15	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	90	--		
t_{fall}	Fall Time	--	30	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1446	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	128	--		
C_{rss}	Reverse Transfer Capacitance	--	13.1	--		
Q_g	Total Gate Charge	--	32	--	nC	V_{DS}=520V I_D=9A V_{GS}=10V (Note:3,4)
Q_{gs}	Gate-to-Source Charge	--	5	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	16	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	9	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	36	A	
V_{SD}	Diode Forward Voltage	--	--	1.4	V	IS=9A,VGS=0V
t_{rr}	Reverse Recovery Time	--	310	--	nS	VGS=0V IS=9A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	4.1	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤1%.

Typical Feature curve T_J = 25°C, unless otherwise noted

Figure1: Output Characteristics

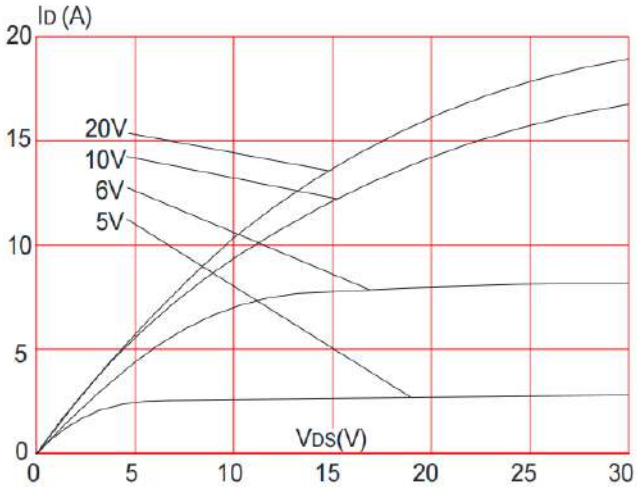


Figure 2: Typical Transfer Characteristics

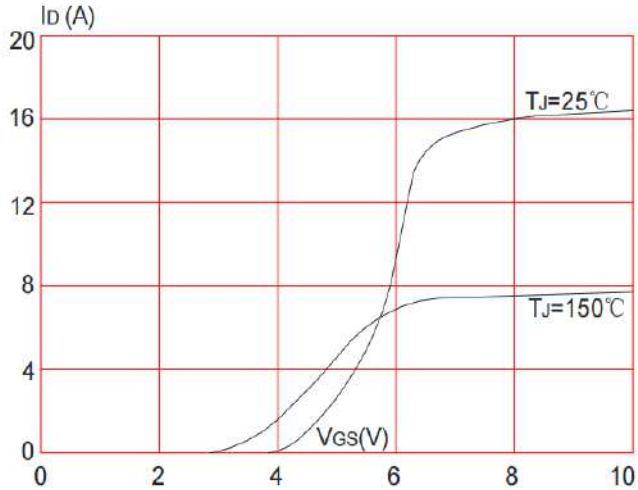


Figure 3: On-resistance vs. Drain Current

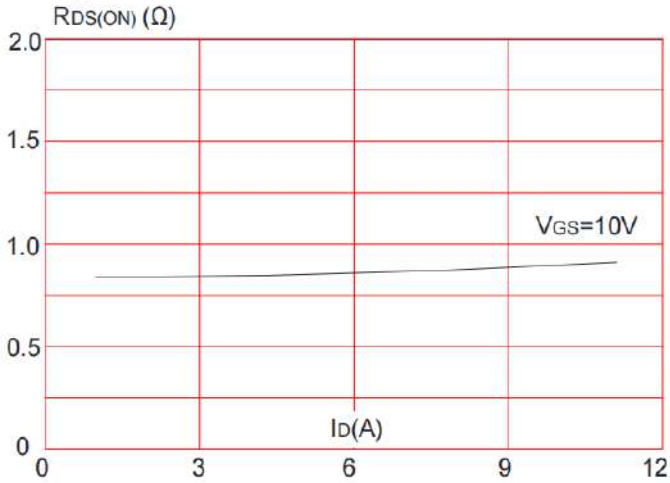


Figure 4: Body Diode Characteristics

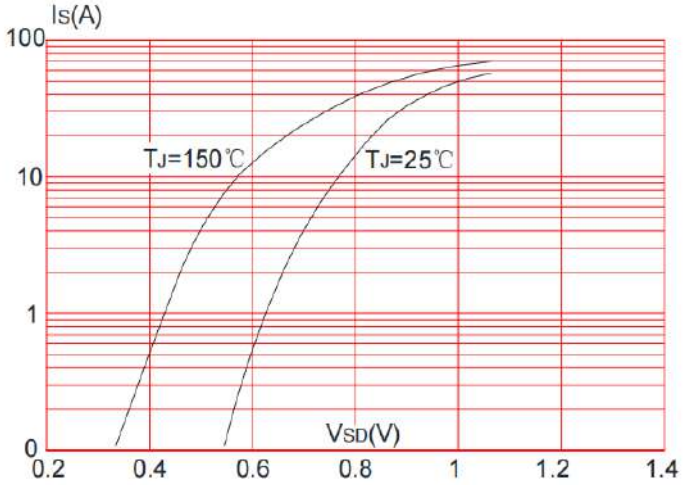


Figure 5: Gate Charge Characteristics

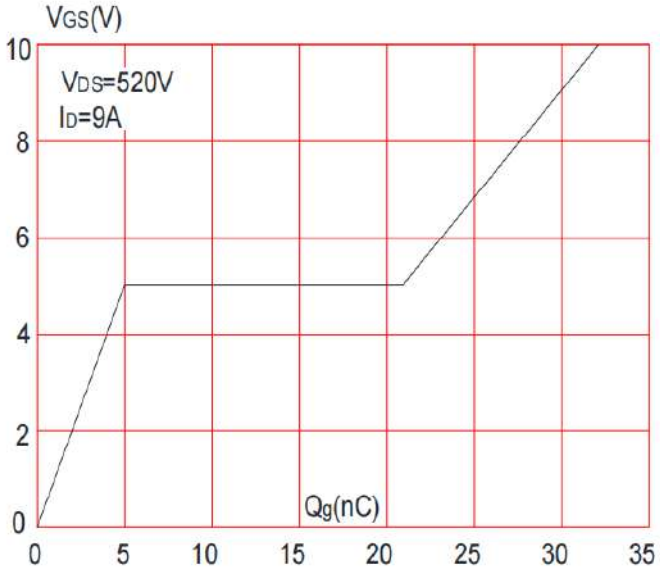


Figure 6: Capacitance Characteristics

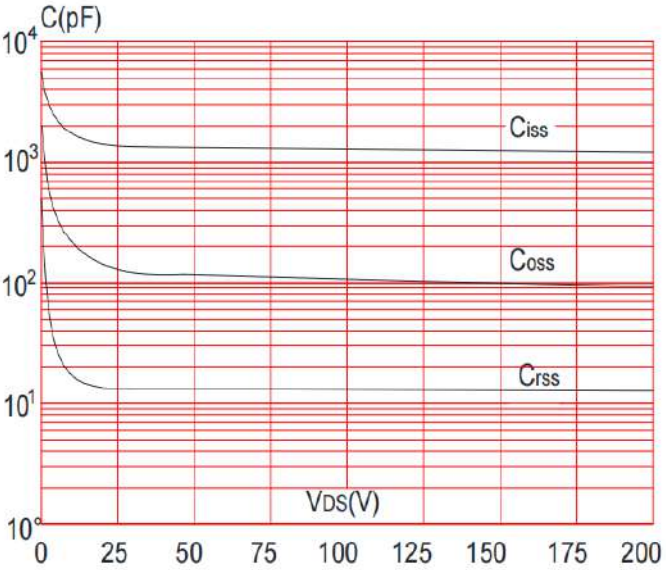


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

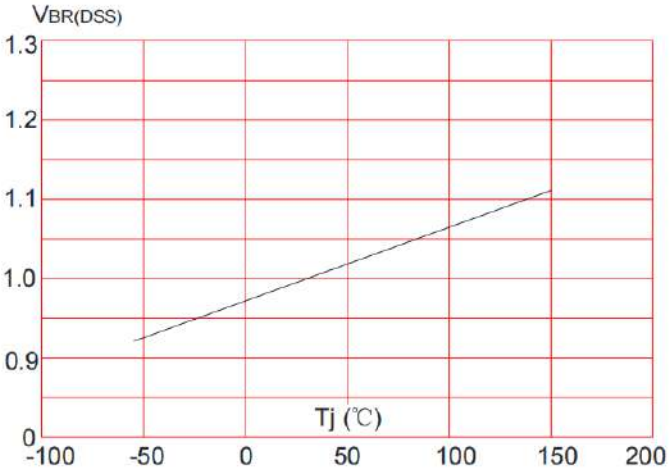


Figure 8: Normalized on Resistance vs. Junction Temperature

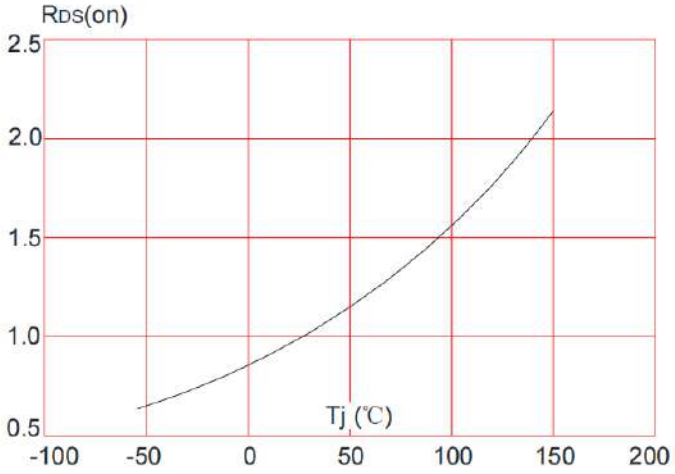


Figure 9: Maximum Safe Operating Area

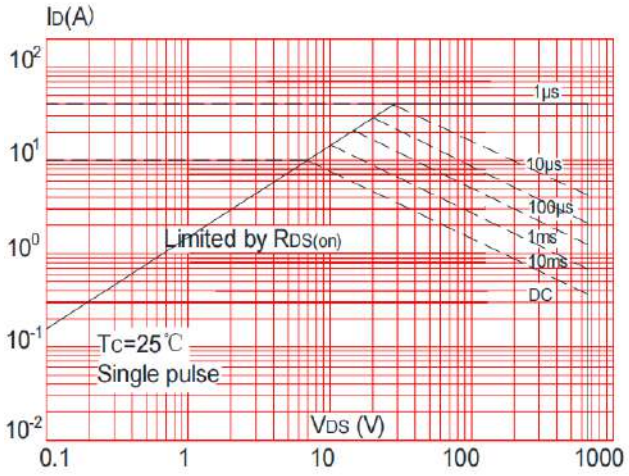


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

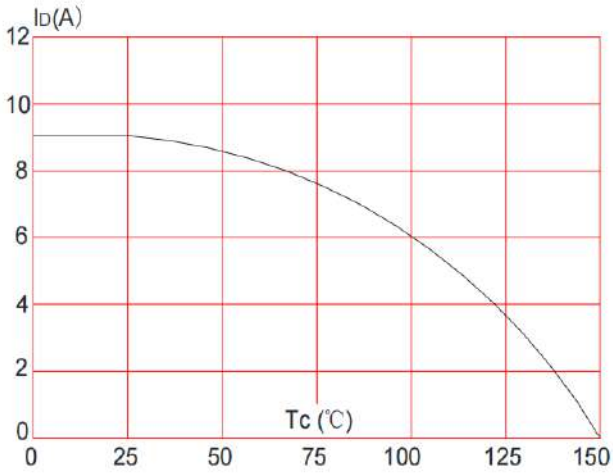
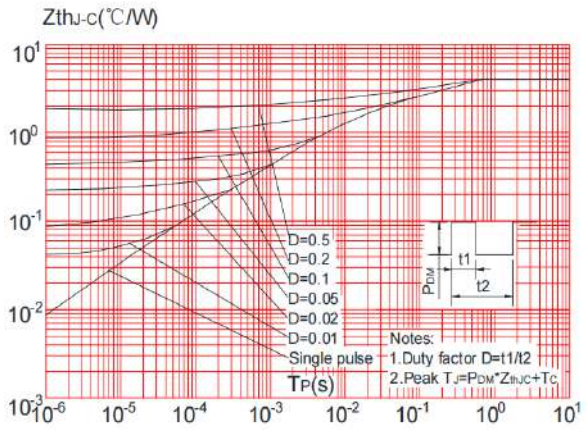


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuits and Waveforms

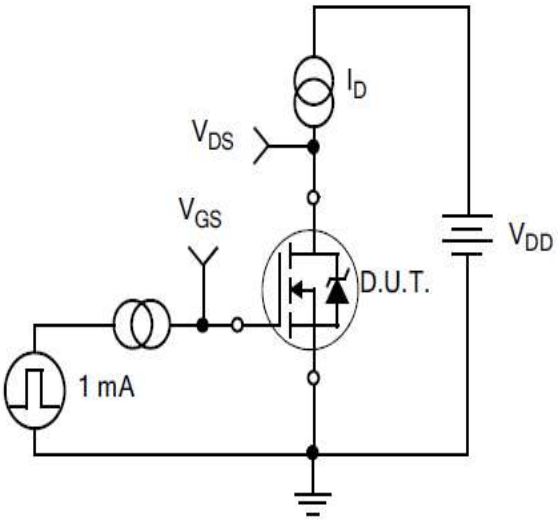


Figure10.
Gate Charge Test Circuit

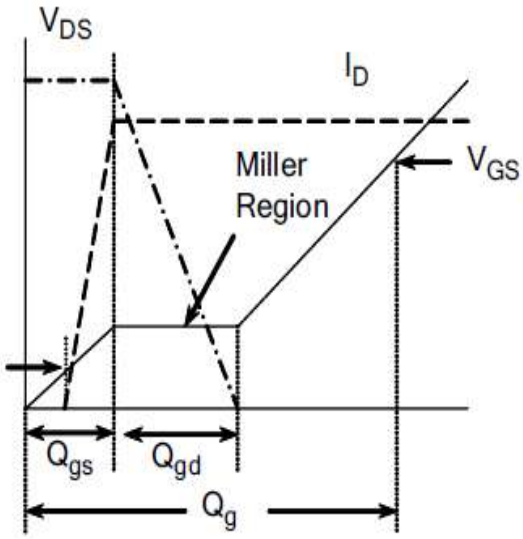


Figure11.
Gate Charge Waveform

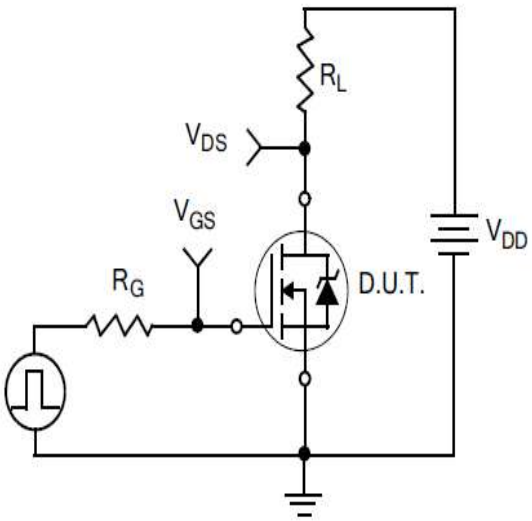


Figure12.
Resistive Switching Test Circuit

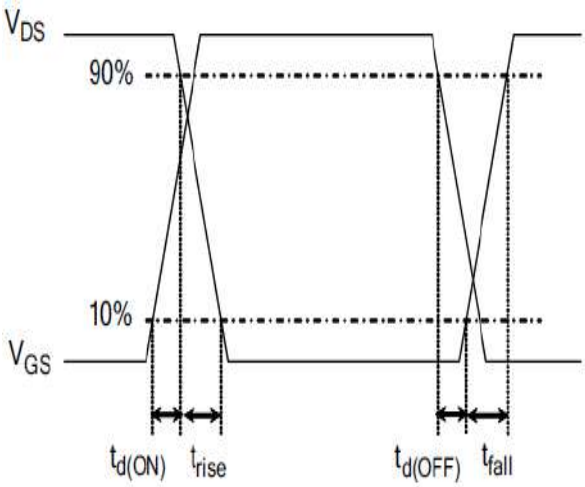


Figure13.
Resistive Switching Waveforms

Test Circuits and Waveforms

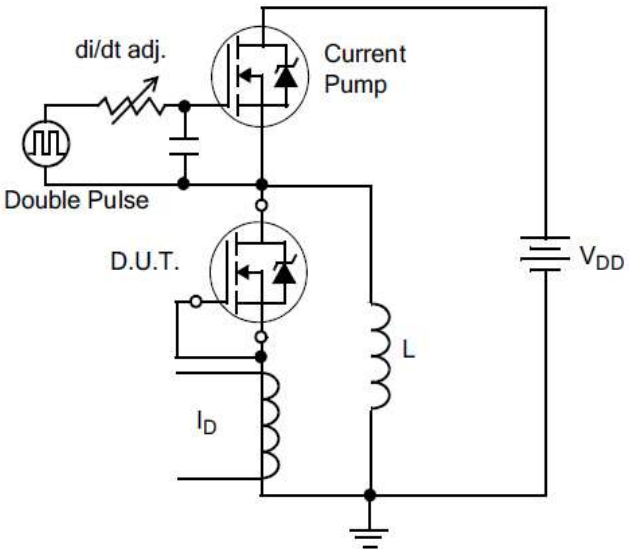


Figure14.Diode Reverse Recovery Test Circuit

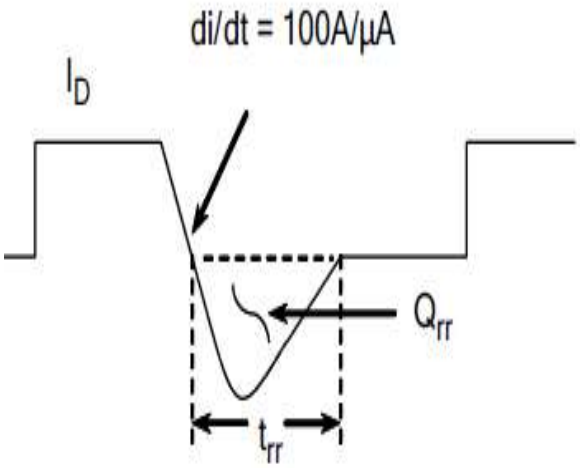


Figure15.Diode Reverse Recovery Waveform

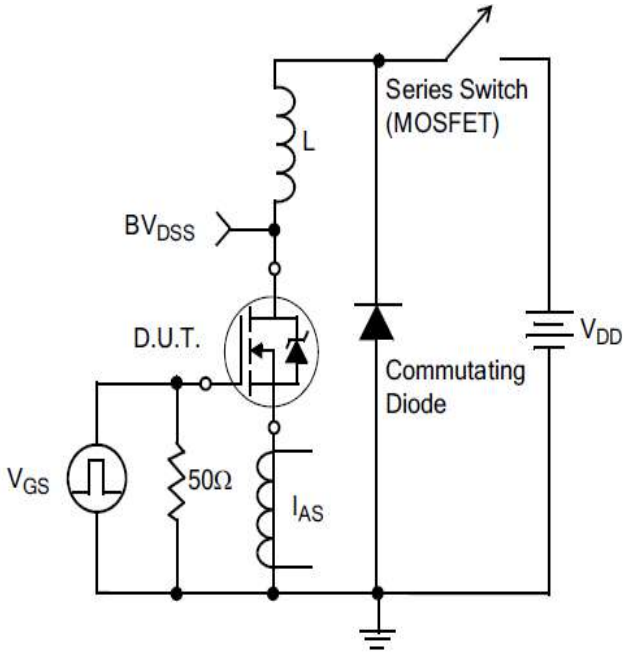
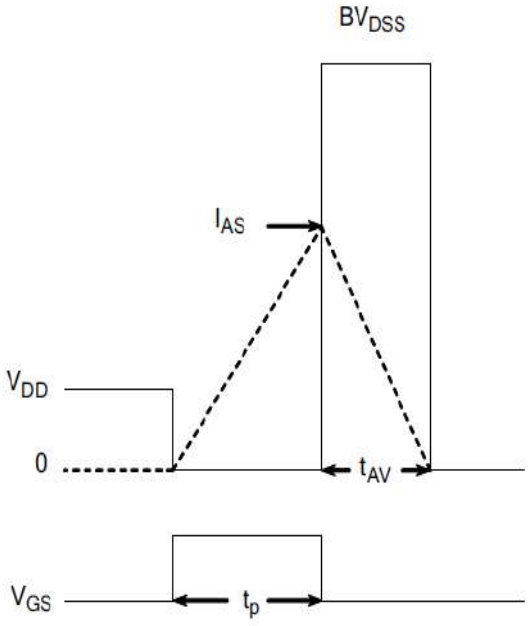


Figure16.Unclamped Inductive Switching Test Circuit

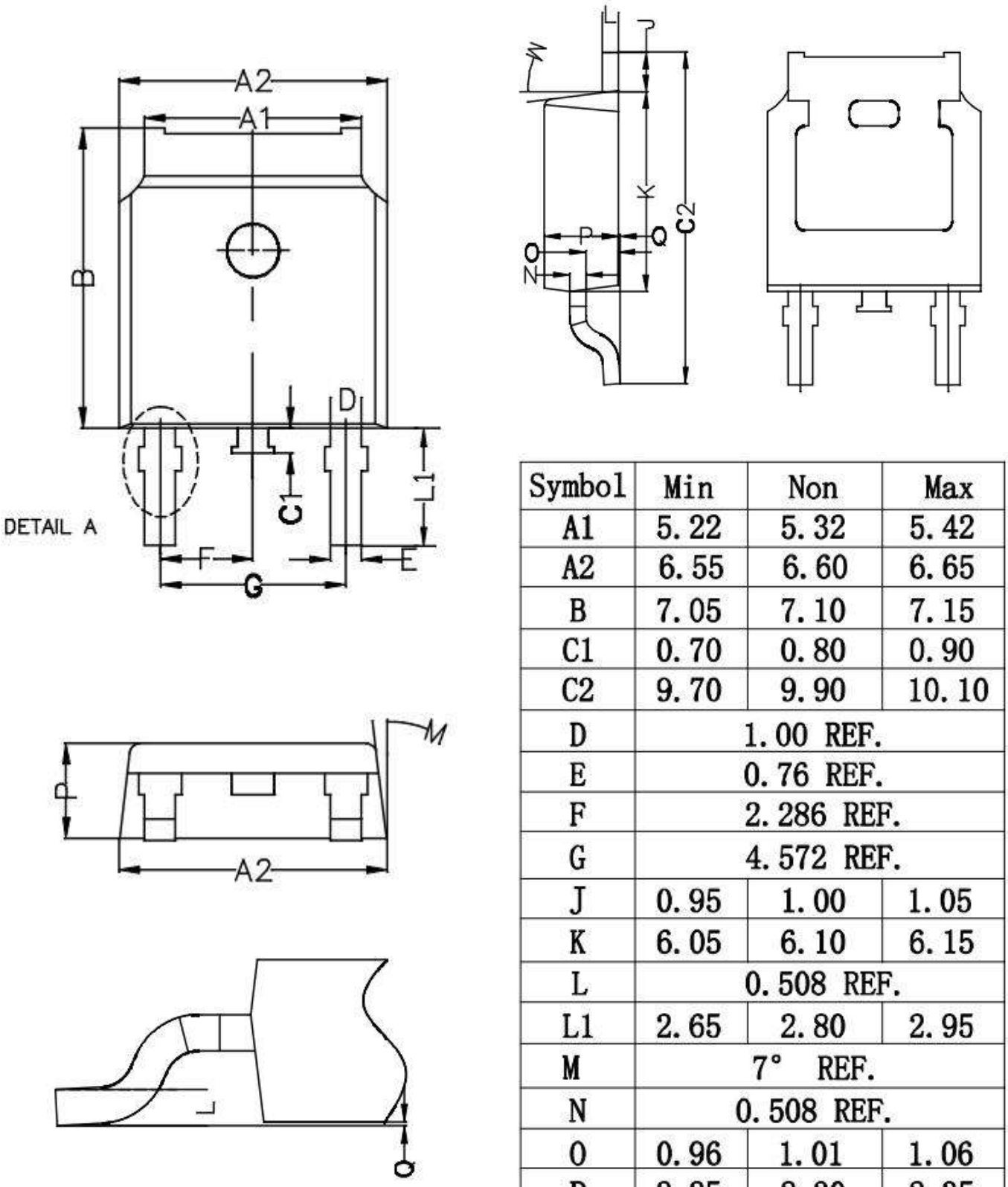


$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure17.Unclamped Inductive Switching Waveforms

Package outline drawing

Unit: mm



Symbol	Min	Non	Max
A1	5.22	5.32	5.42
A2	6.55	6.60	6.65
B	7.05	7.10	7.15
C1	0.70	0.80	0.90
C2	9.70	9.90	10.10
D	1.00 REF.		
E	0.76 REF.		
F	2.286 REF.		
G	4.572 REF.		
J	0.95	1.00	1.05
K	6.05	6.10	6.15
L	0.508 REF.		
L1	2.65	2.80	2.95
M	7° REF.		
N	0.508 REF.		
O	0.96	1.01	1.06
P	2.25	2.30	2.35
Q	0.00	0.05	0.10

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