

N Channel MOSFET

P6)

Lead Free Package and Finish

Applications:

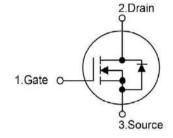
- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- •PFC stages for server & telecom
- •Consumer

lo	Rds(ON)(Typ.)	VDSS
9A	0.65Ω	500V

Features:

- •New revolutionary high voltage technology
- •Better RDS(on) in TO-252
- •Ultra Low Gate Charge cause lower driving requirements
- •Periodic avalanche rated
- •Ultra low effective capacitances





Ordering Information

Part Number	Package	Marking
RS9N50D	TO-252	RS9N50D

NOT TO Scale

Symbol	Parameter	RS9N50D	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current (TC = 25℃)	9	
ID	Continuous Drain Current (TC = 100℃)	6.8	Α
ldм	Pulsed Drain Current (Note*1)	40.0	
PD	Power Dissipation(Tc=25℃)	70.0	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy (Note*2)	320	mJ
IAR	Avalanche Current (Note*1)	8.0	Α
EAR	Repetitive Avalanche Engergy (Note*1)	45	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	$^{\circ}\! \mathbb{C}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

^{*}Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS9N50D	Units	Test Conditions
RθJC	Junction-to-Case	1.78	°C/W	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	60		1 cubic foot chamber,free air.



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RS9N50D

OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	500			V	VGS = 0V, ID = 250µA, TJ= 25℃
			500		V	VGS = 0V, ID = 250µA, TJ= 150℃
IDSS	Drain-to-Source Leakage Current			1.0	μA	VDS=500V,VGS=0V
1000	Gate-to-Source Forward Leakage			100		VGS=+30V VDS=0V
IGSS	Gate-to-Source Reverse Leakage			-100 nA		VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		0.65	0.80	Ω	VGS=10V,ID=4.5A
VGS(TH)	Gate Threshold Voltage	3.0		4.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		23			VDS=400V
trise	Rise Time		15			ID=9A
td(OFF)	Turn-OFF Delay Time		90		ns	RG=25Ω
tfall	Fall Time		30			VGS=10V

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		1056			VGS=0V
Coss	Output Capacitance		105		pF	VDS=100V
Crss	Reverse Transfer Capacitance		4.4			f=1.0MHz
Qg	Total Gate Charge		22.0			VDS=480V
Qgs	Gate-to-Source Charge		5.0		nC	ID=9A
Qgd	Gate-to-Drain("Miller") Charge		9.0			VGS=10V

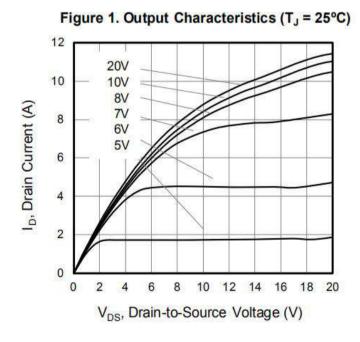
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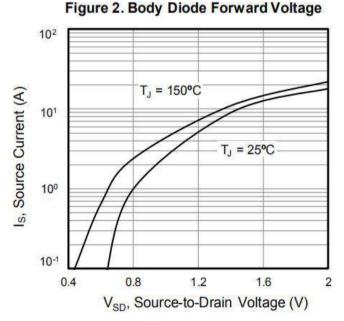


Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current		-	9	Α	Integral pn-diode
ISM	Maximum Pulsed Current			40	Α	in MOSFET
VSD	Diode Forward Voltage		0.6	1.4	V	IS=9A,VGS=0V Tj=25℃
trr	Reverse Recovery Time		310		nS	VD 050VVV00 0V
Qrr	Reverse Recovery Charge		4.1		μC	VR=250V,VGS=0V IS=9A,di/dt=100A/µs
Irrm	Peak Reverse Recovery Current		30		Α	10 σπ,απατ 100π υμο

Notes:





^{*1.}Repetitive rating; pulse width limited by maximum junction temperature.

^{*2.} Pulse width tp limited by Tj,max



Figure 3. Drain Current vs. Temperature

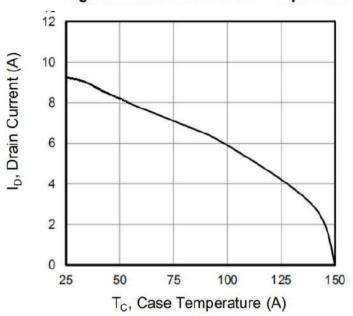


Figure 4. BV_{DSS} Variation vs. Temperature

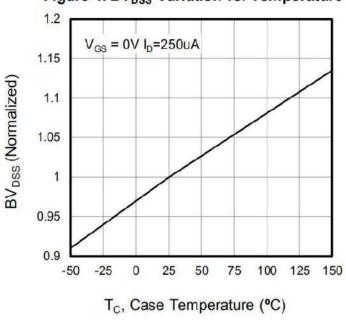


Figure 5. Transfer Characteristics

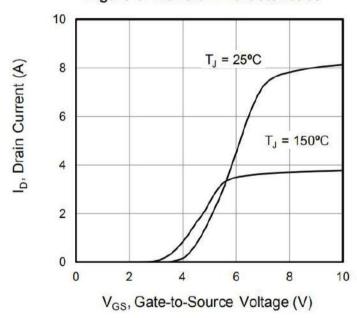
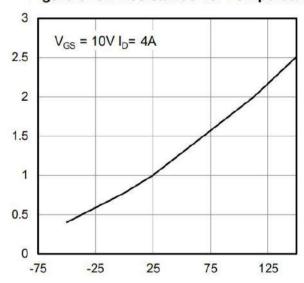


Figure 6. On-Resistance vs. Temperature



T_J, Junction Temperature (°C)

RDS(on), On-Resistance (Normalized)



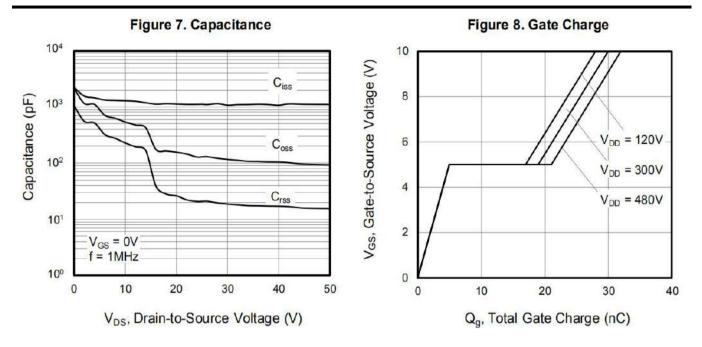


Figure 9. Transient Thermal Impedance TO-252 10¹ Z_{thJC}, Thermal Impedance (K/W) 100 10-1 D = 0.5D = 0.2D = 0.110-2 D = 0.05D = 0.02D = 0.0110-3 Single Pulse 10-4 10-7 10-6 10-5 10-4 10-3 10-2 10-1 Tp, Pulse Width (s)



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

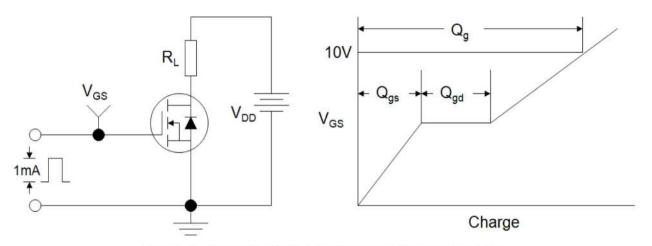


Figure B: Resistive Switching Test Circuit and Waveform

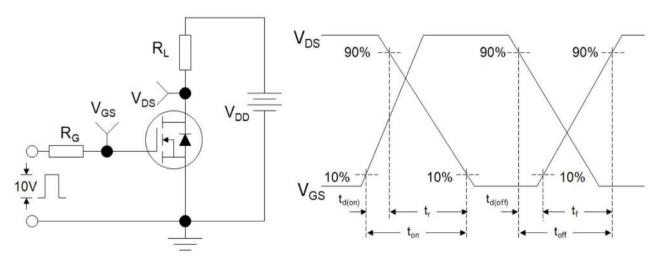
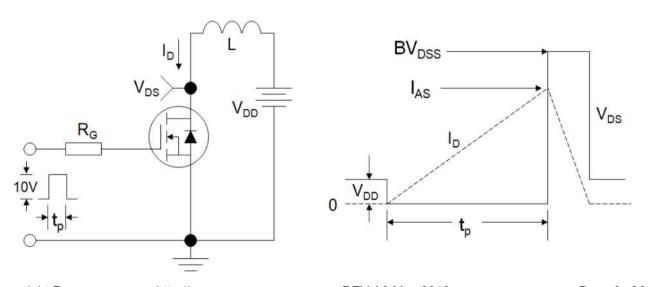


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



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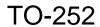
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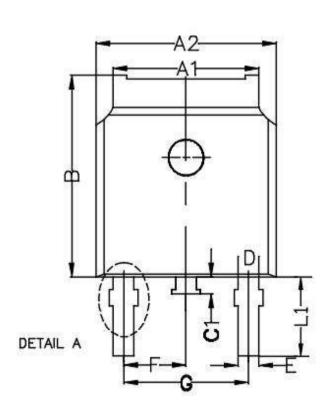
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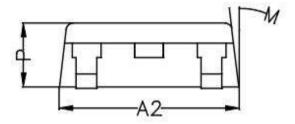
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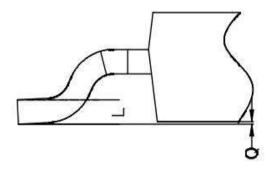


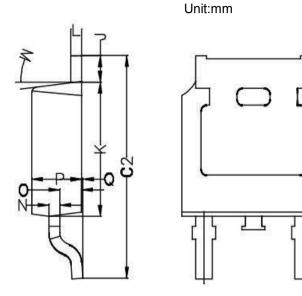
Package outline drawing











Symbol	Min	Non	Max			
A1	5. 22	5. 32	5. 42			
A2	6. 55	6.60	6.65			
В	7.05	7. 10	7. 15			
C1	0.70	0.80	0.90			
C2	9. 70	9.90	10. 10			
D		1.00 REF.	Ē.			
Е		0.76 REF	•			
F	2. 286 REF.					
G	12	4. 572 RE	F.			
J	0.95	1.00	1.05			
K	6.05	6. 10	6. 15			
L		0.508 RE	F.			
L1	2.65	2.80	2. 95			
М		7° REF.				
N	0. 508 REF.					
0	0.96	1. 01	1.06			
P	2. 25	2.30	2. 35			
Q	0.00	0.05	0.10			



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