REASUNOS

RS85N150T

N-Channel Enhancement Mode MOSFET

Lead Free Package and Finish

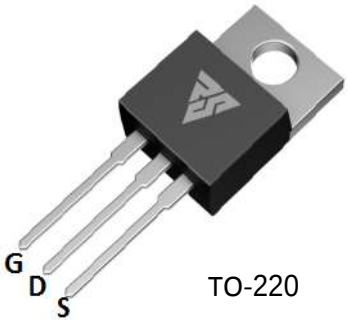
I_D	$R_{DS(ON)}$(Max.)	V_{DSS}
150A	3.6mΩ	85V

Applications:

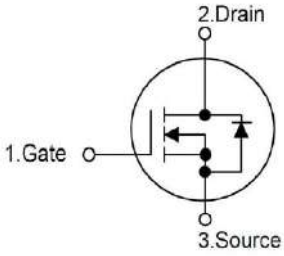
- BMSsystem
- LCDMappliances
- High power inverter system

Features:

- V_{DS}=85V; ID=150A@ VGS=10V
- $R_{DS(ON)}$<3.6mΩ @ V_{GS}=10V
- SuperTrench
- High UIS and UIS 100% Test
- RoHS Compliant



TO-220



Not to Scale

Ordering Information

Part Number	Package	Marking
RS85N150T	TO-220	RS85N150T

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS85N150T	Units
VDSS	Drain-to-Source Voltage	85	V
ID	Continuous Drain Current（Tc=25℃）	150	A
	Continuous Drain Current Tc=100℃	140	
IDM	Pulsed Drain Current (Note*1)	600	
PD	Power Dissipation（Tc=25℃）	310	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy (Note*2)	750	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS85N150T	Units	Test Conditions
RθJC	Junction-to-Case	0.5	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	85	--	--	V	VGS=0V,ID=250μA
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	VDS=100V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+20V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	2.8	3.6	mΩ	VGS=10V,ID=75A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	37	--	nS	VDS=43V ID=60A VGS=10V RL=4.7Ω RG=0.72Ω
trise	Rise Time	--	63	--		
td(OFF)	Turn-OFF Delay Time	--	78	--		
tfall	Fall Time	--	41	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	7447	--	pF	VGS=0V VDS=43V f=100KHz
Coss	Output Capacitance	--	1075	--		
Crss	Reverse Transfer Capacitance	--	43	--		
Qg	Total Gate Charge	--	130	--	nC	VDS=68V ID=60A VGS=10V
Qgs	Gate-to-Source Charge	--	40	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	39	--		

Source-Drain Diode Characteristics

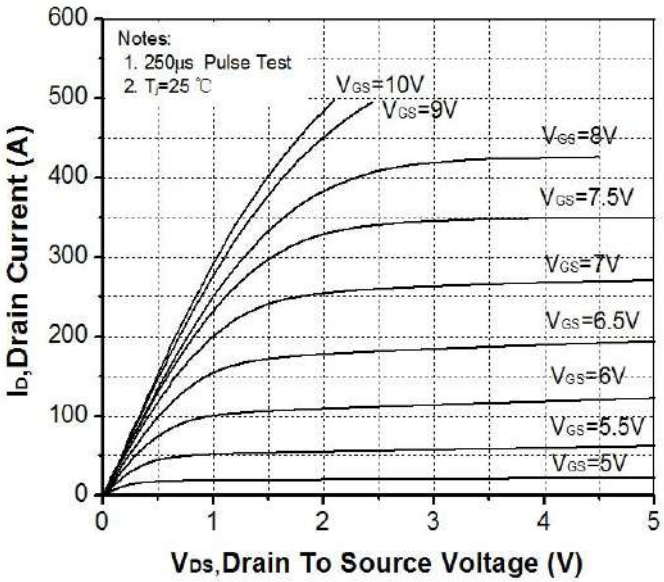
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{SD}	Source-Drain Current(Body Diode)	--	150	--	A	
I_{SDM}	Pulsed Source-Drain Current(Body Diode)		600	--	A	
V_{SD}	Diode Forward Voltage (Note*3)	--	--	1.4	V	IS=60A,VGS=0V
trr	Reverse Recovery Time (Note*3)	--	56	--	nS	VGS=0V I_F=60A,di/dt=100A/μs
Qrr	Reverse Recovery Charge (Note*3)	--	84	--	nC	

Notes:

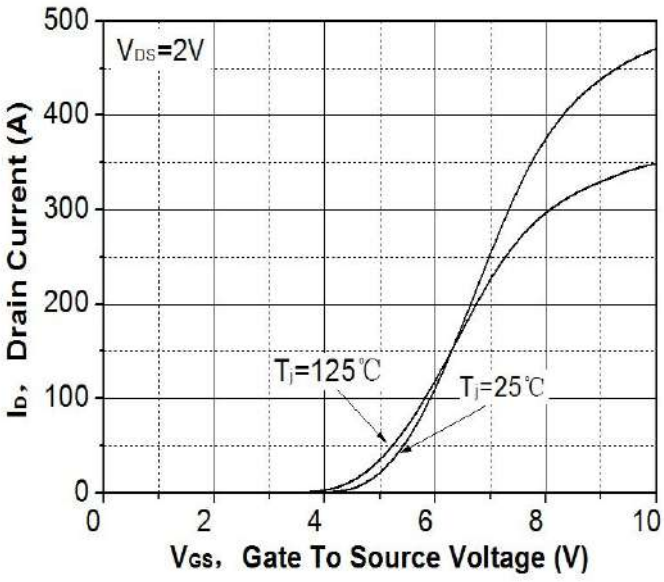
*1.Repetitive Rating: Pulse width limited by maximum junction temperature
*2.E_{AS} condition:T_J=25℃,L=0.5mH,I_{AS}=55A
*3.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting T_J=25℃

Typical Feature curve

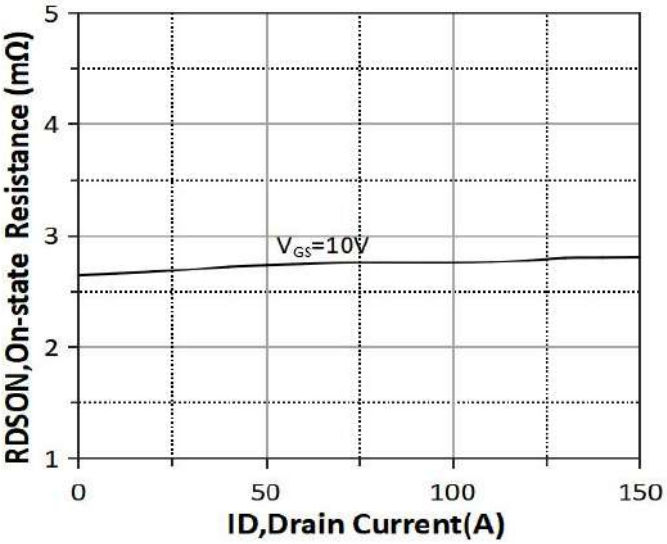
On-state characteristics



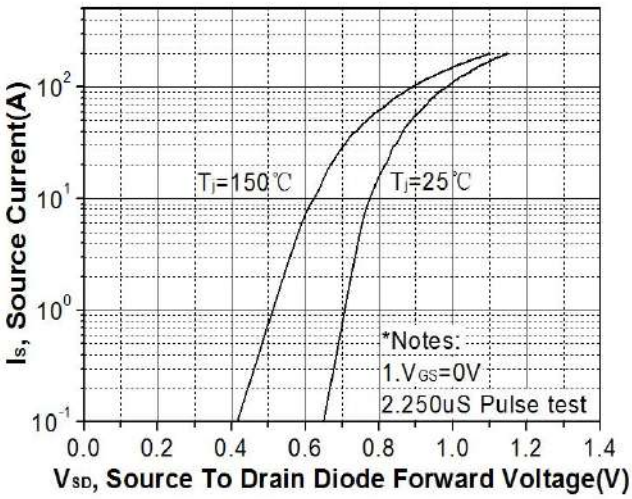
Transfer Characteristics



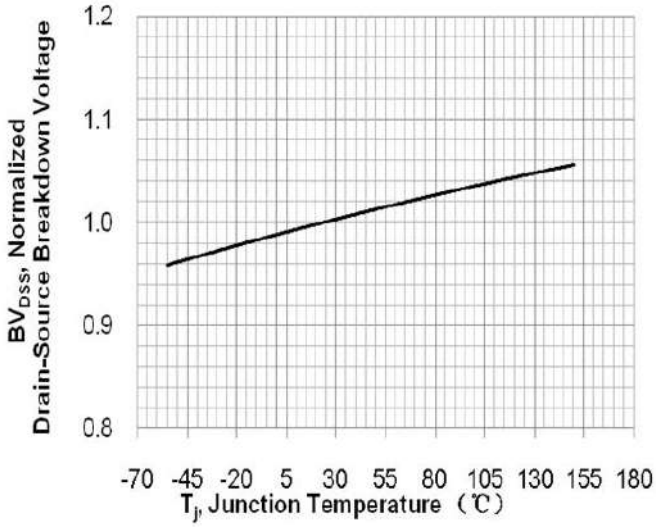
On-resistance variation vs.drain current and gate voltage



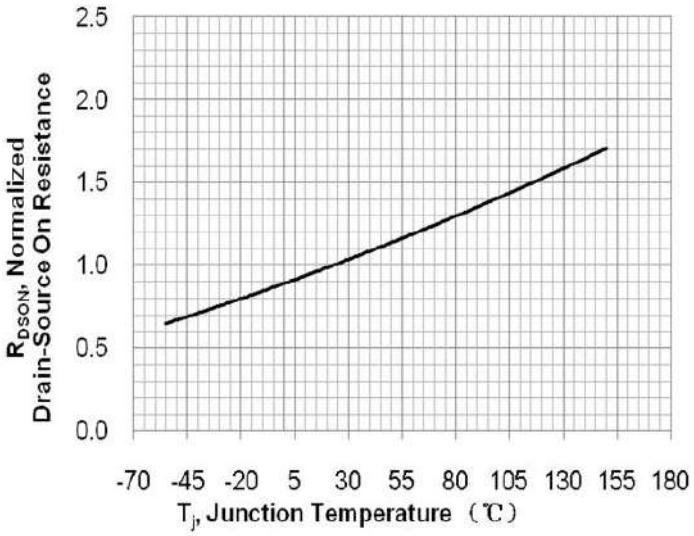
On-state current vs.diode forward voltage



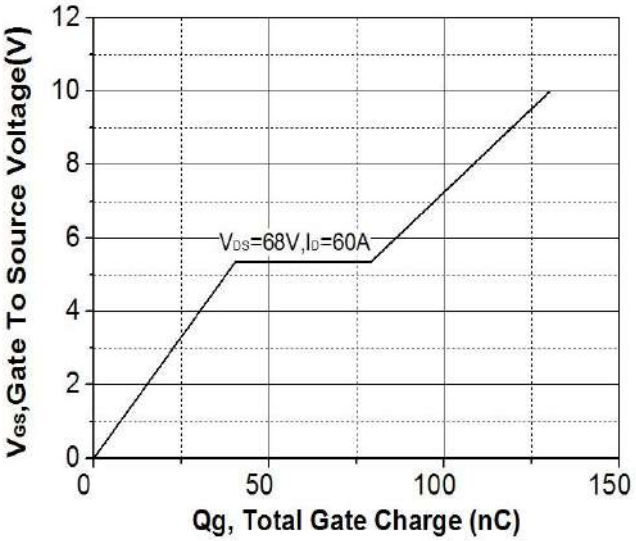
Breakdown voltage variation vs.junction temperature



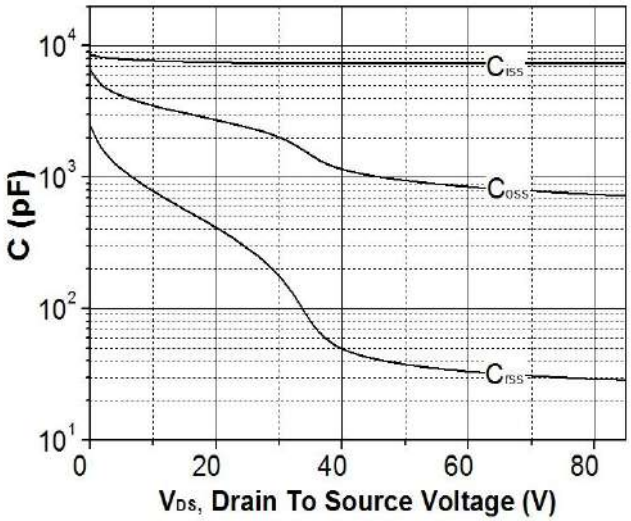
On-resistance variation vs.junction temperature



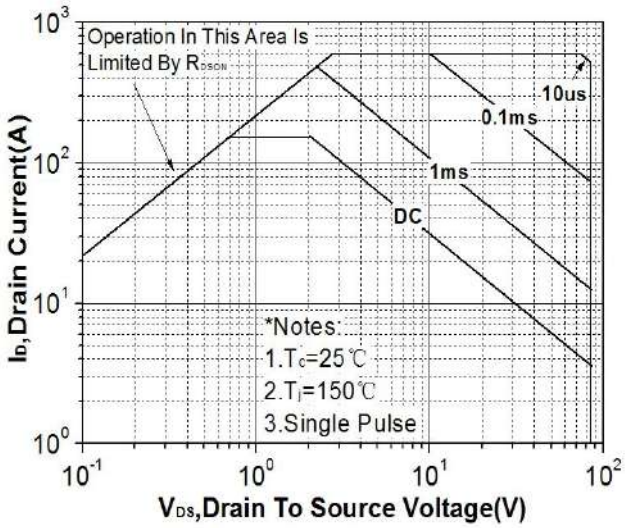
Gate charge characteristics



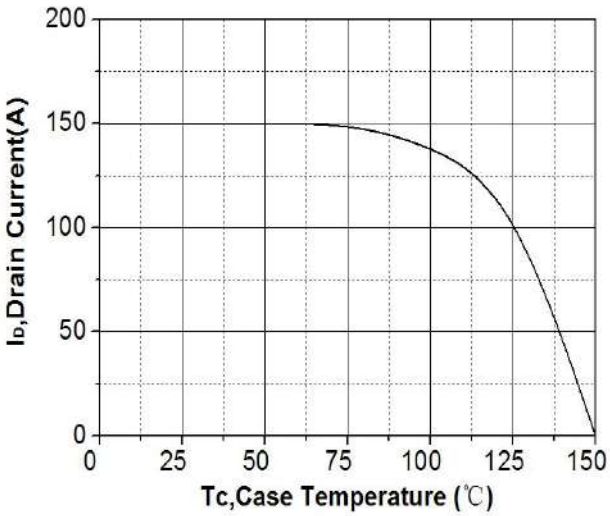
Capacitance characteristics



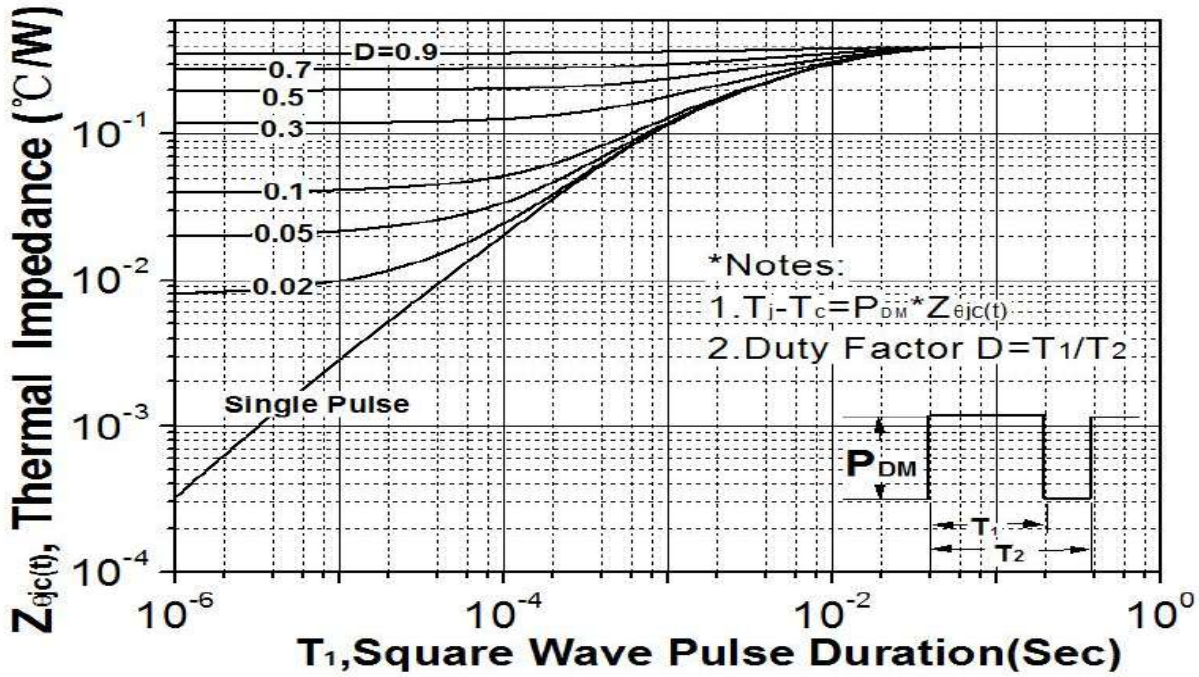
Maximum safe operating area



Maximum drain current vs.case temperature



Transient thermal response curve



Test Circuits and Waveforms

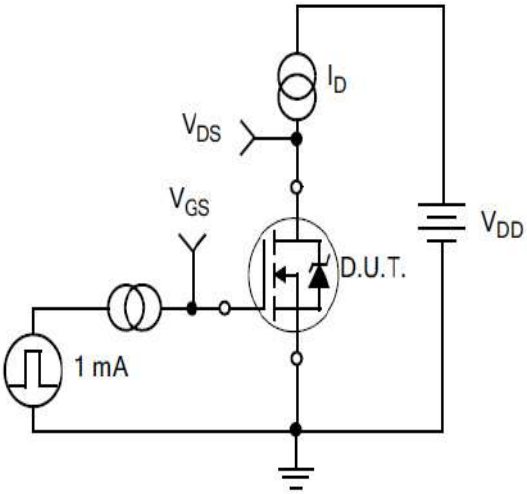


Figure A.
Gate Charge Test Circuit

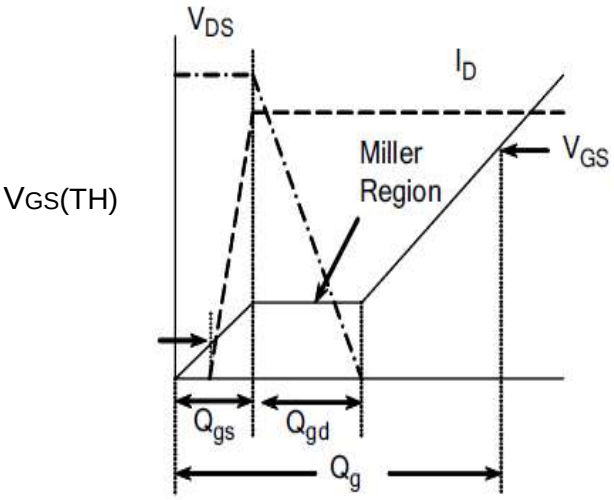


Figure B.
Gate Charge Waveform

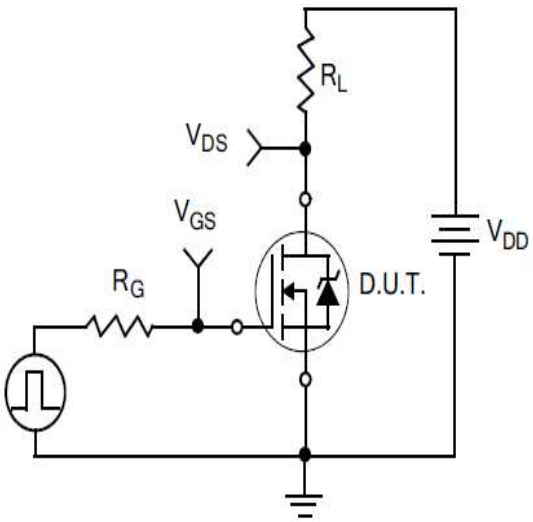


Figure C.
Resistive Switching Test Circuit

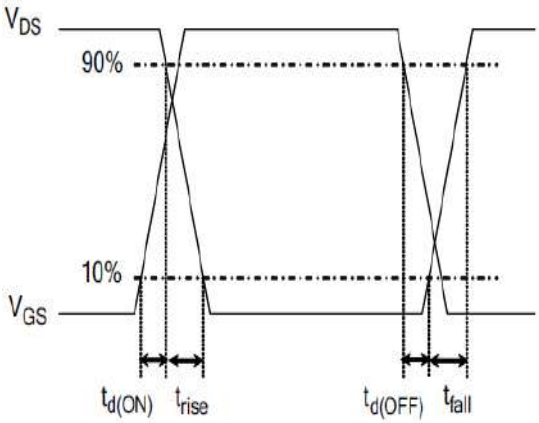


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

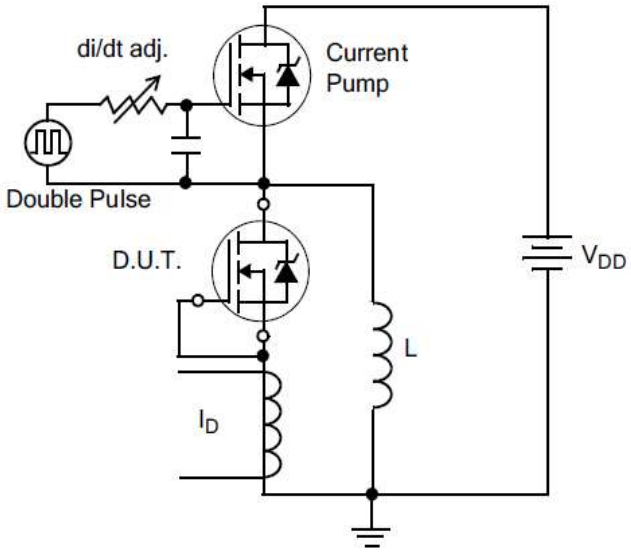


Figure E.Diode Reverse Recovery Test Circuit

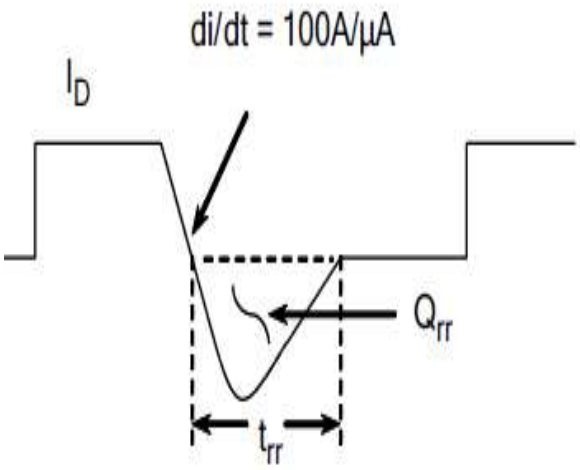


Figure F.Diode Reverse Recovery Waveform

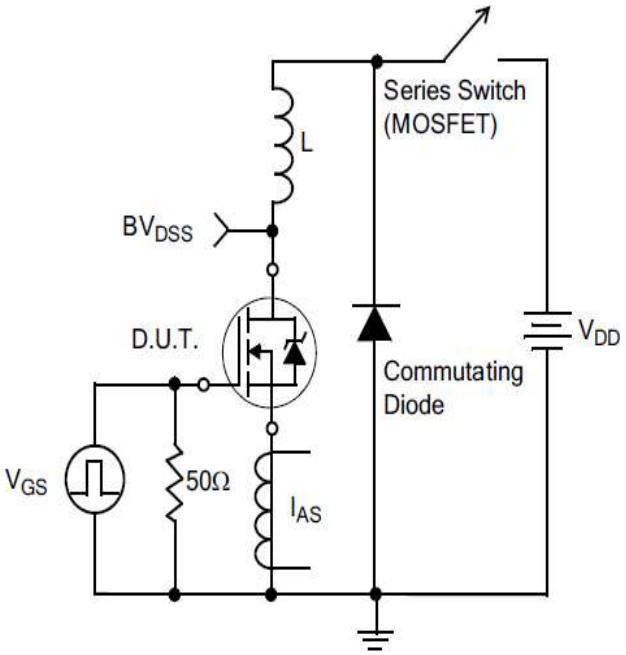
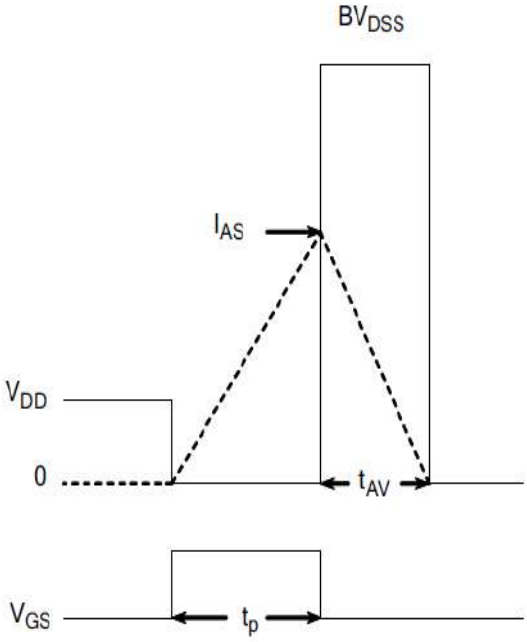


Figure G.Unclamped Inductive Switching Test Circuit

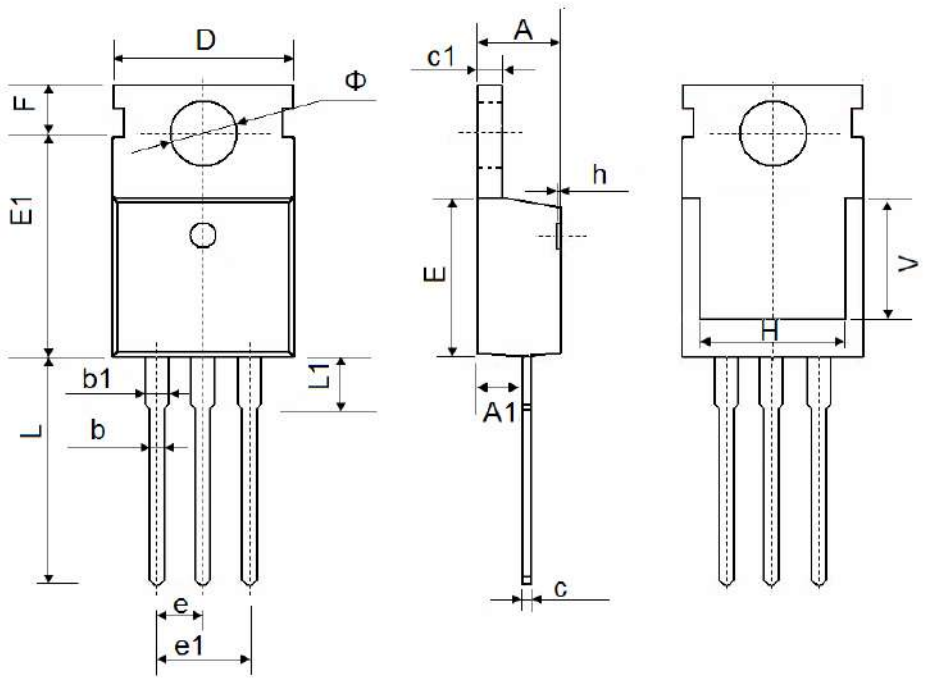


$$E_{AS}= \frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing

Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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