

REASUNOS**RS85N150S****N-Channel Enhancement Mode MOSFET**

Lead Free Package and Finish

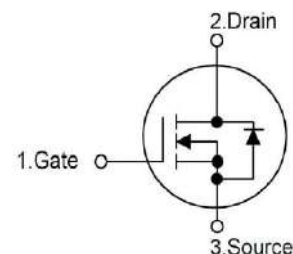
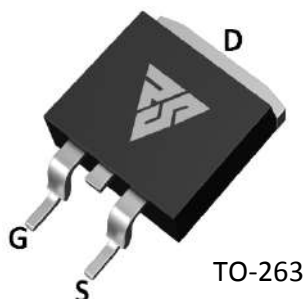
Applications:

- BMSsystem
- LCDMappliances
- High power inverter system

ID	R _{DS(ON)} (Max.)	V _{DSS}
150A	3.4mΩ	85V

Features:

- V_{DS}=85V; I_D=150A @ V_{GS}=10V
- R_{DS(ON)}<3.4mΩ @ V_{GS}=10V
- SuperTrench
- Surface-mounted package
- High UIS and UIS 100% Test
- RoHS Compliant



Not to Scale

Ordering Information

Part Number	Package	Marking
RS85N150S	TO-263	RS85N150S

Absolute Maximun Ratings Tc=25°C unless otherwise specified

Symbol	Parameter	RS85N150S	Units
V _{DSS}	Drain-to-Source Voltage	85	V
I _D	Continuous Drain Current (T _c =25°C)	150	A
	Continuous Drain Current T _c =100°C	140	
I _{DM}	Pulsed Drain Current (Note*1)	600	
PD	Power Dissipation (T _c =25°C)	310	W
V _{GS}	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy (Note*2)	750	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
T _J and T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS85N150S	Units	Test Conditions
R _{θJC}	Junction-to-Case	0.5	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150°C.

REASUNOS**RS85N150S****OFF Characteristics** TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	85	--	--	V	VGS=0V, ID=250μA
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	VDS=85V, VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+20V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	2.8	3.4	mΩ	VGS=10V, ID=75A
VGS(TH)	Gate Threshold Voltage	2.0	--	4.0	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	37	--	nS	VDS=43V ID=60A VGS=10V RL=4.7Ω RG=0.72Ω
trise	Rise Time	--	63	--		
td(OFF)	Turn-OFF Delay Time	--	78	--		
tfall	Fall Time	--	41	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	7447	--	pF	VGS=0V VDS=43V f=100KHz
Coss	Output Capacitance	--	1075	--		
Crss	Reverse Transfer Capacitance	--	43	--		
Qg	Total Gate Charge	--	130	--	nC	VDS=68V ID=60A VGS=10V
Qgs	Gate-to-Source Charge	--	40	--		
Qgd	Gate-to-Drain("Miller") Charge	--	39	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
ISD	Source-Drain Current(Body Diode)	--	150	--	A	
ISDM	Pulsed Source-Drain Current(Body Diode)		600	--	A	
VSD	Diode Forward Voltage (Note*3)	--	--	1.4	V	IS=60A,VGS=0V
trr	Reverse Recovery Time (Note*3)	--	56	--	nS	VGS=0V
Qrr	Reverse Recovery Charge (Note*3)	--	84	--	nC	IF=60A,di/dt=100A/μs

Notes:

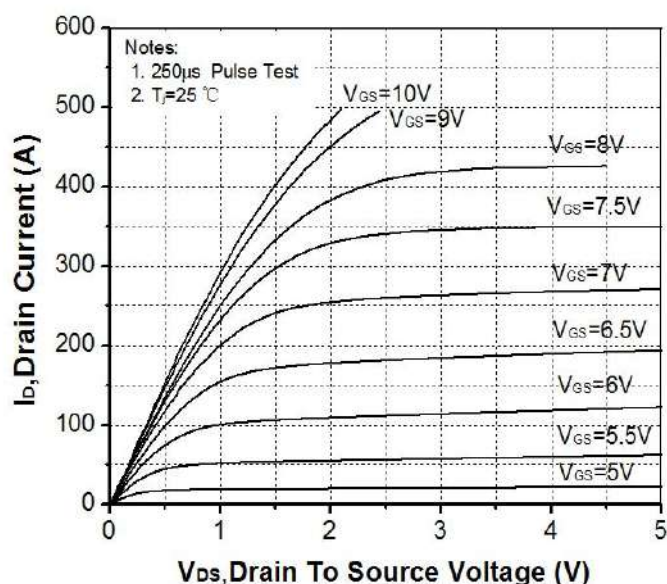
*1.Repetitive Rating: Pulse width limited by maximum junction temperature

*2.EAS condition:TJ=25℃,L=0.5mH,IAS=55A

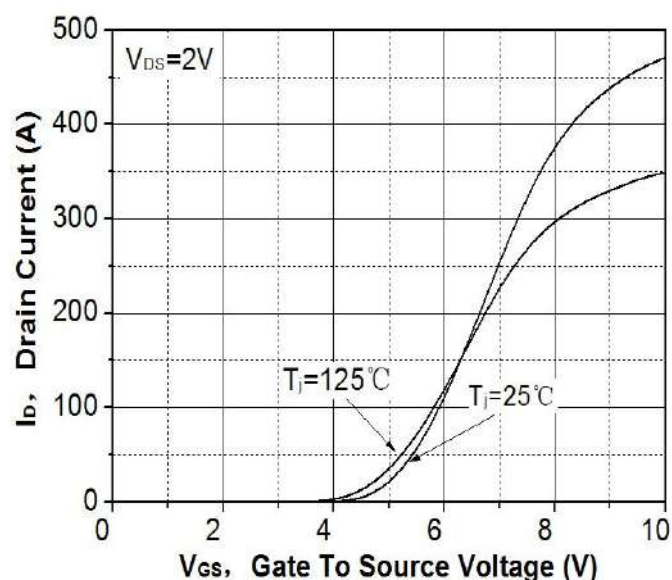
*3.Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1.5\%$, RG=25Ω, Starting TJ=25℃

Typical Feature curve

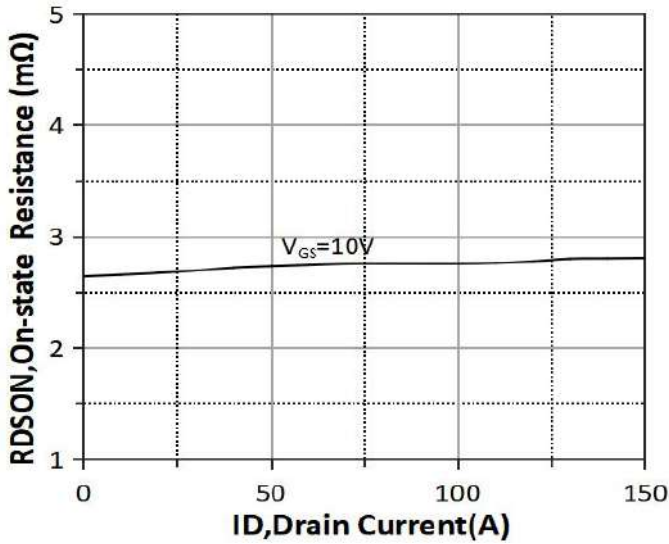
On-state characteristics



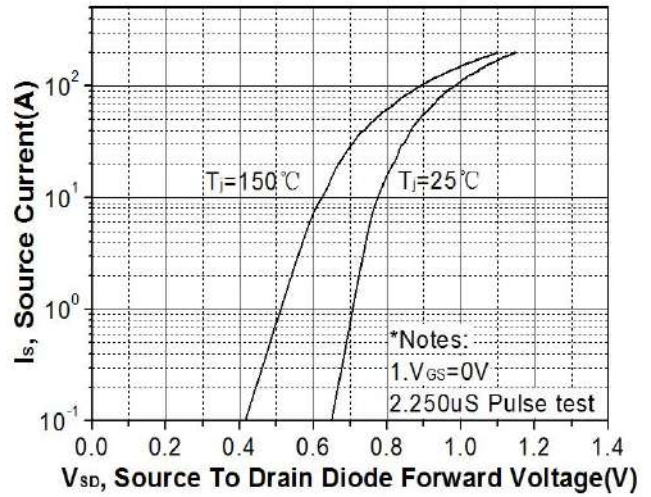
Transfer Characteristics



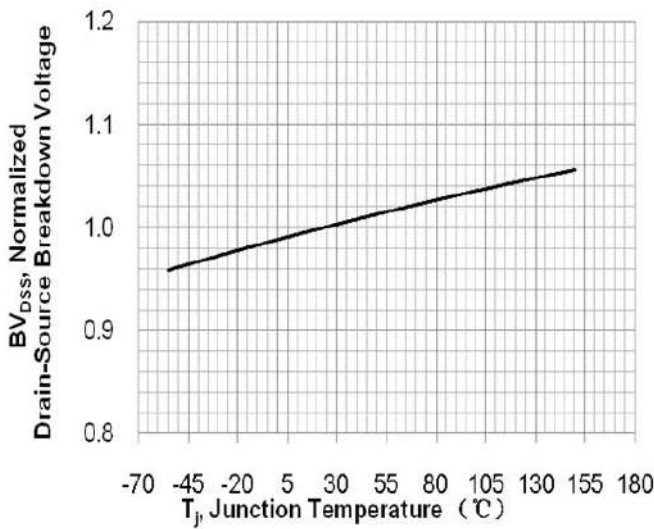
On-resistance variation vs. drain current and gate voltage



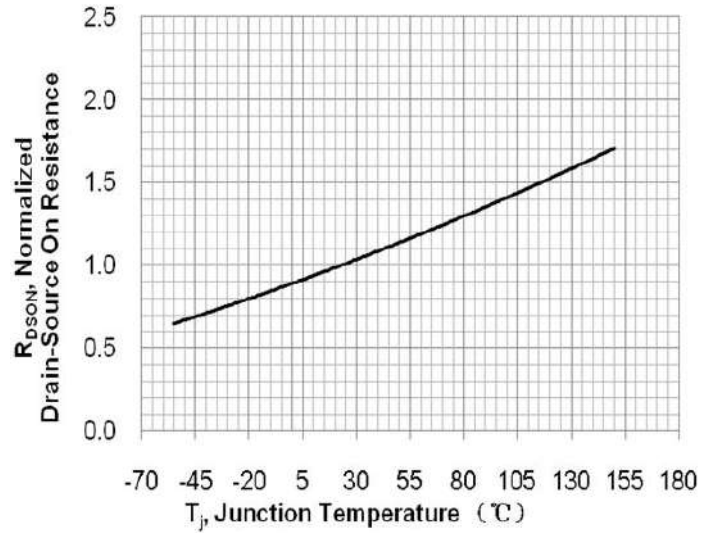
On-state current vs. diode forward voltage



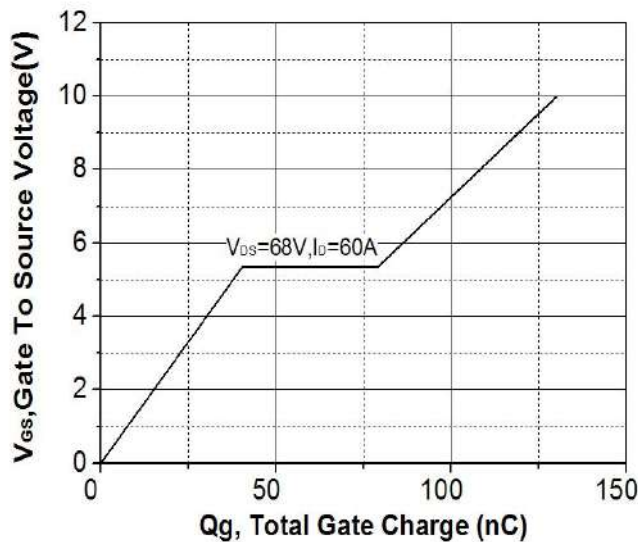
Breakdown voltage variation vs. junction temperature



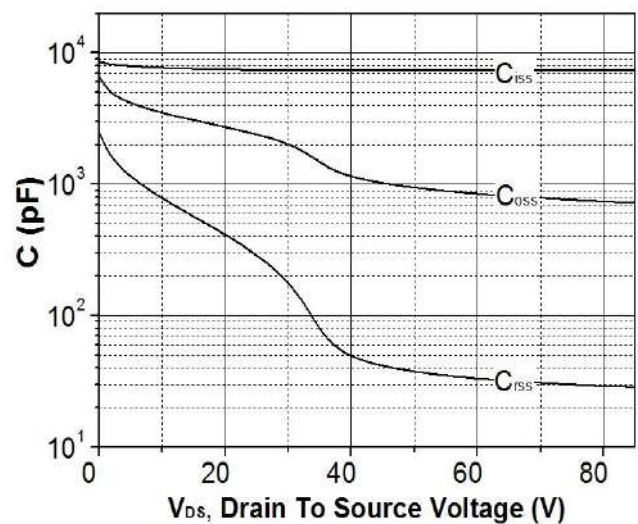
On-resistance variation vs. junction temperature



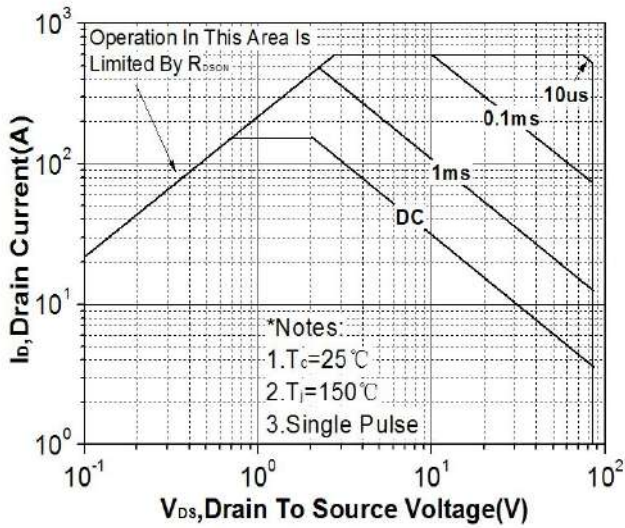
Gate charge characteristics



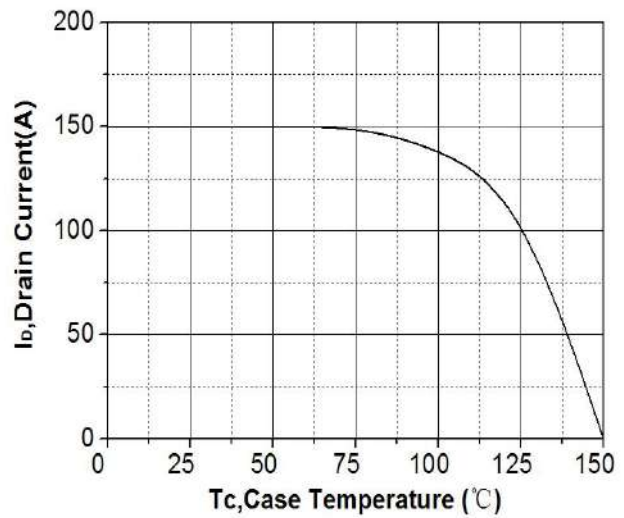
Capacitance characteristics



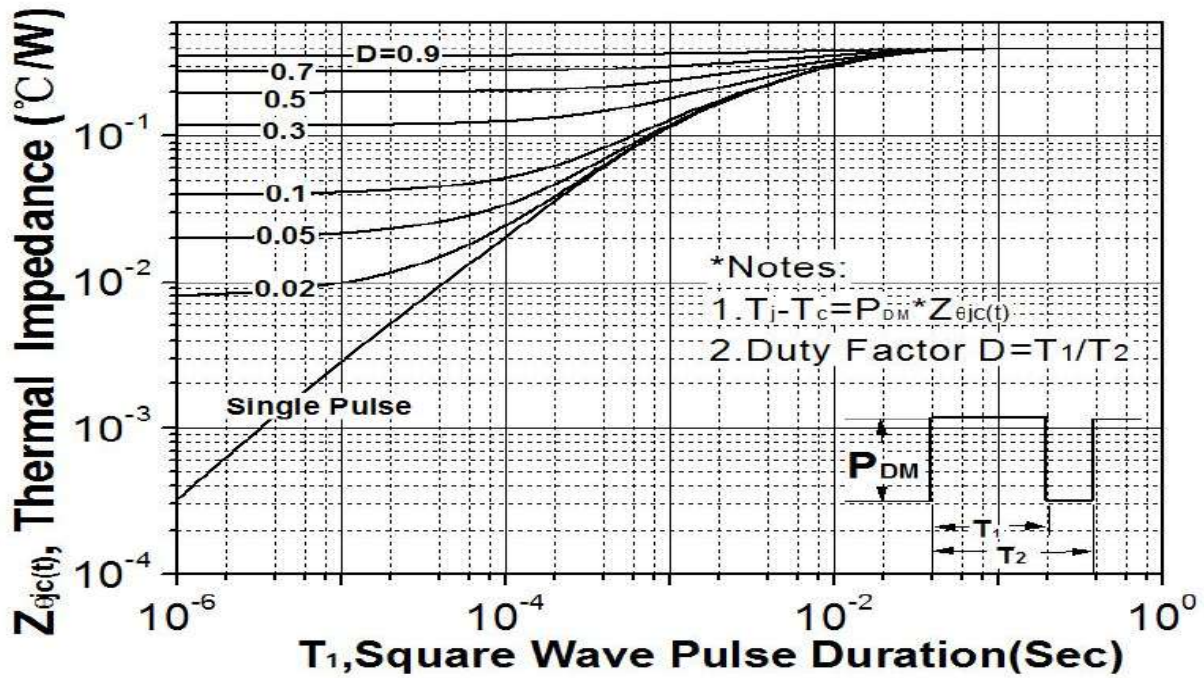
Maximum safe operating area



Maximum drain current vs. case temperature



Transient thermal response curve



Test Circuits and Waveforms

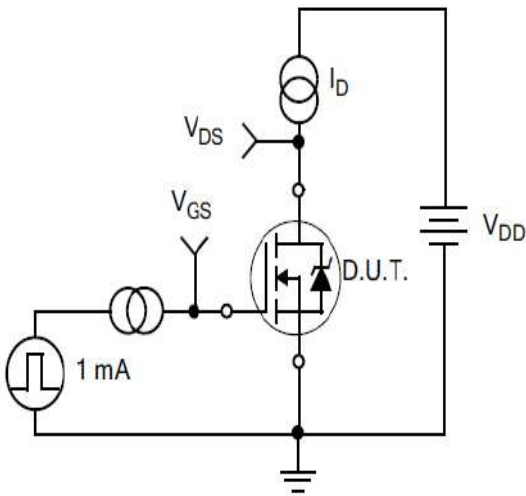


Figure A.
Gate Charge Test Circuit

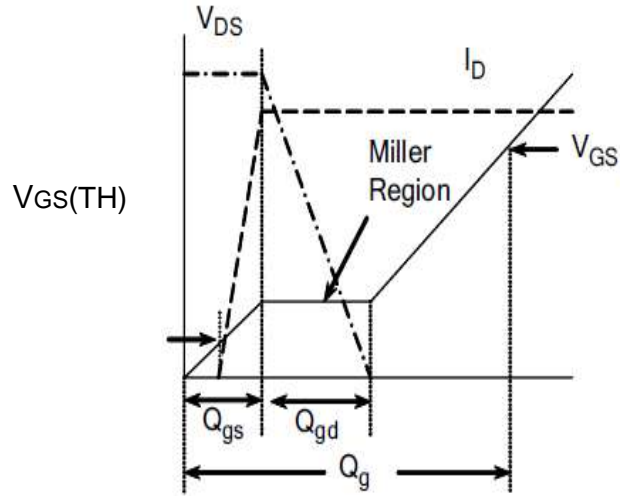


Figure B.
Gate Charge Waveform

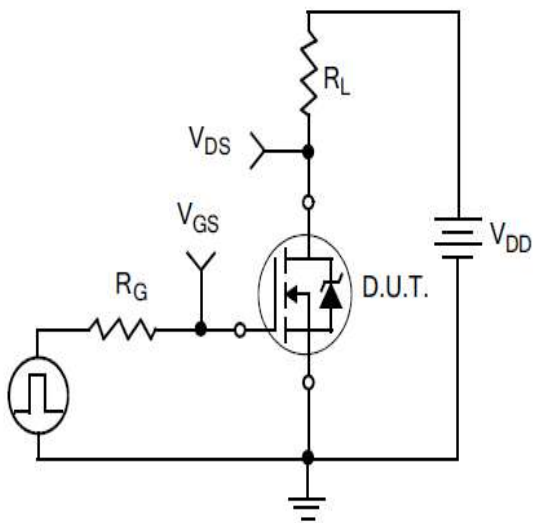


Figure C.
Resistive Switching Test Circuit

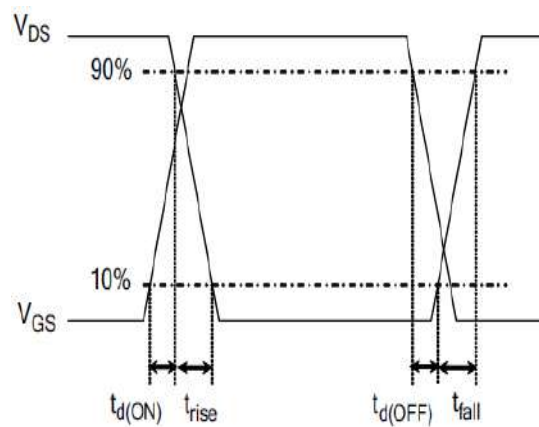


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

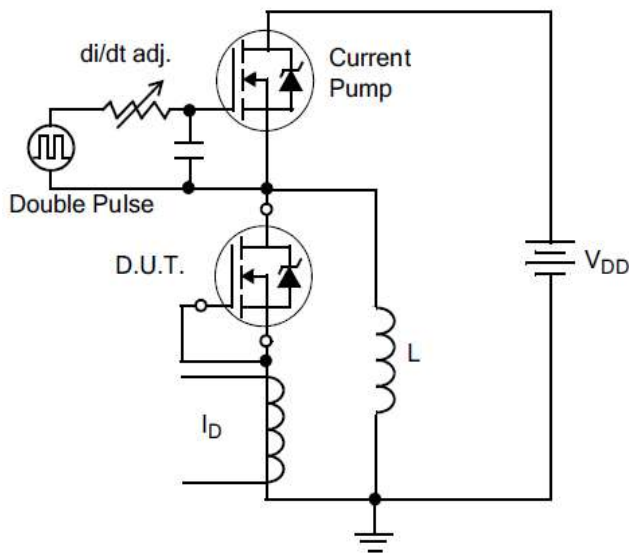


Figure E. Diode Reverse Recovery Test Circuit

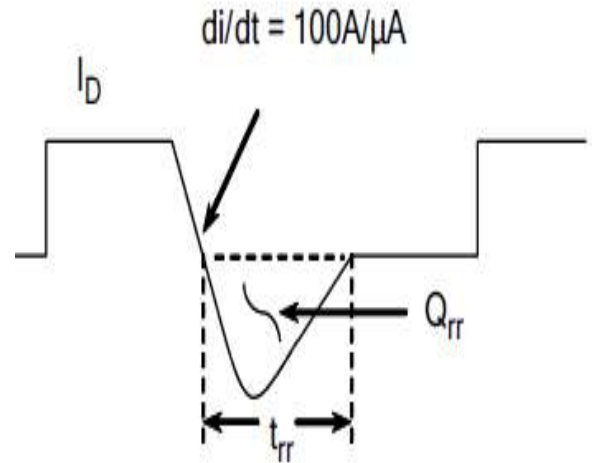


Figure F. Diode Reverse Recovery Waveform

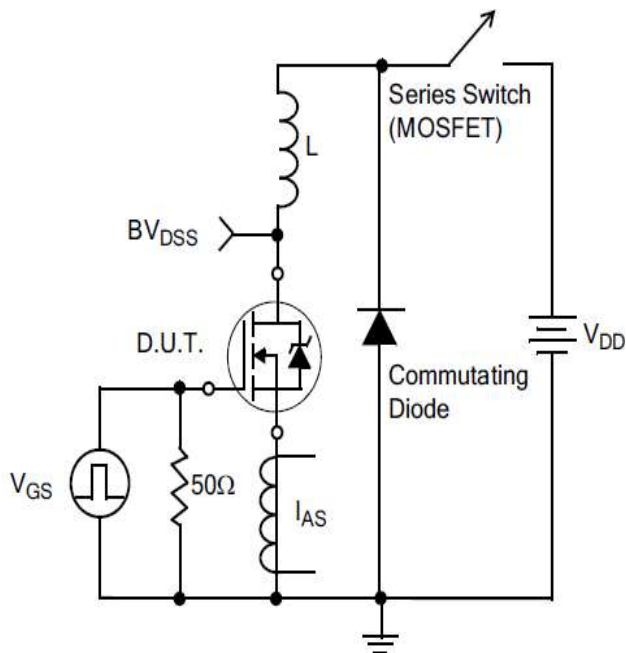
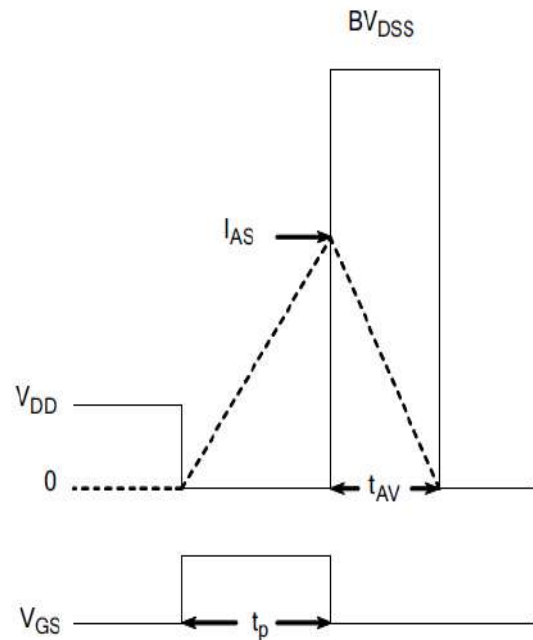


Figure G. Unclamped Inductive Switching Test Circuit

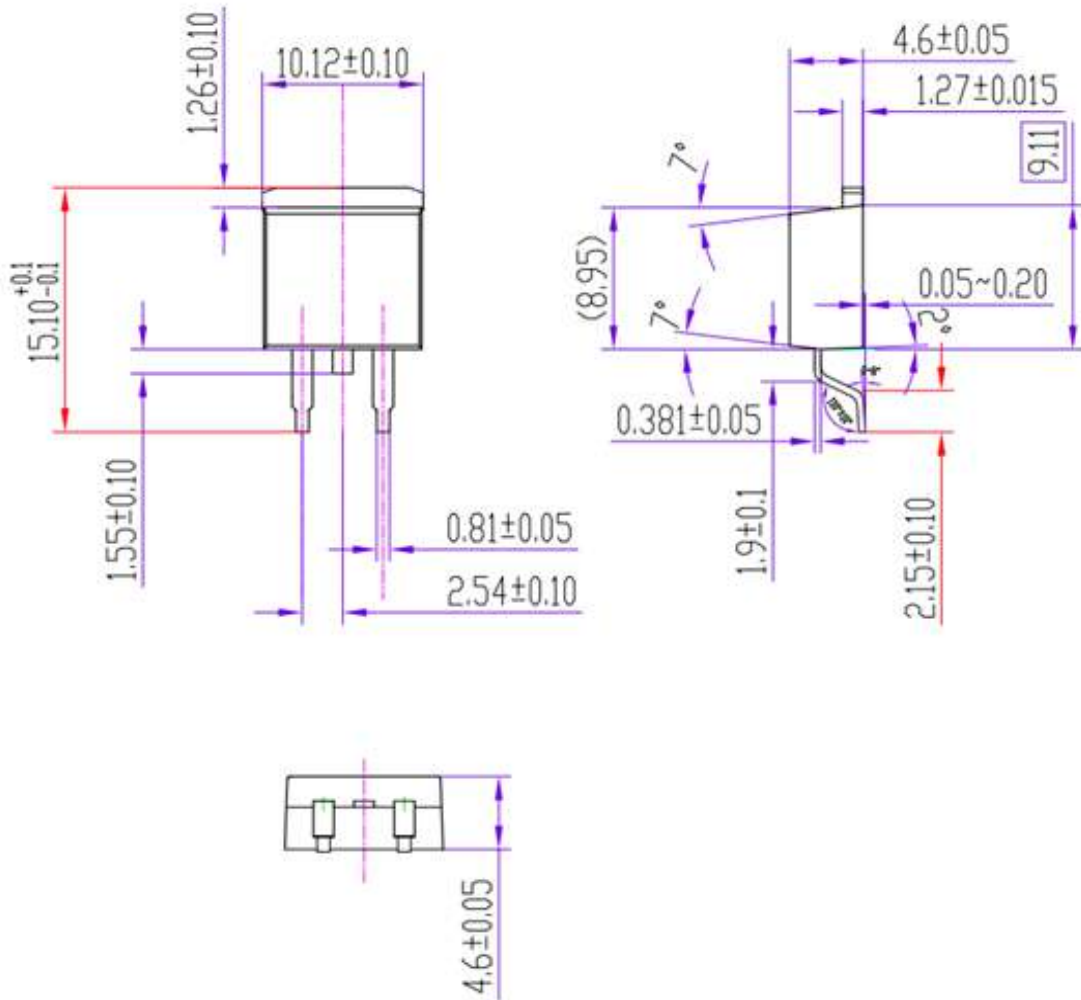


$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing

Unit:mm



TO-263

Disclaimers:

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the specifications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights,nor the rights of others.Reproduction of information in Reasunos's data sheets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warranties for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

- 1.Life support devices or systems are devices or systems which:
 - a.are intended for surgical implant into the human body,
 - b.support or sustain life,
 - c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.
 - 2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.
-