

# **N** Channel MOSFET

#### Applications:

- Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

#### Features:

- •Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

#### Ordering Information

Part Number	Package	Marking
RS7N65F	TO-220F	RS7N65F

Not to Scale

ID

7A

#### Absolute Maximun Ratings Tc=25°C unless otherwise specified

Symbol	Parameter	RS7N65F	Units
VDSS	Drain-to-Source Voltage (Note*1)	650	V
ID	Continuous Drain Current	7.0	
ID@ 100 ℃	Continuous Drain Current	4.5	А
ldм	Pulsed Drain Current (Note*2)	28.0	
PD	Power Dissipation	97	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH VDD=50V RG=25Ω Starting TJ=25℃	250	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	°C
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

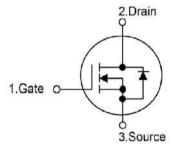
\*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

#### **Thermal Resistance**

Symbol	Parameter	RS7N65F	Units	Test Conditions
Rejc	Junction-to-Case	1.29		Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
Reja	Junction-to-Ambient	60		1 cubic foot chamber, free air.







RDS(ON)(Typ.)

1.1Ω

RS7N65F

VDSS

650V



# **OFF Characteristics** TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650			V	Vgs=0V,Id=250µA
Idss	Drain-to-Source Leakage Current			1.0	μA	V <sub>DS</sub> =650V,VGS=0V
	Gate-to-Source Forward Leakage			100	n۸	VGS=+30V VDS=0V
IGSS	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

# ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IRDS(on)	Static Drain-to-Source On-Resistance (Note*3)		1.1	1.4	Ω	V <sub>GS</sub> =10V,I <sub>D</sub> =3.5A
VGS(TH)	Gate Threshold Voltage	3.0		4.0	V	Vgs=Vds,Id=250µA

# Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		18			Vps=325V
trise	Rise Time		19		nS	ID=7A
td(OFF)	Turn-OFF Delay Time		82		115	RG <b>=25</b> Ω
tfall	Fall Time		35			(Note:3,4)

# **Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		997			VGS=0V
Coss	Output Capacitance		97		pF	VDS=25V
Crss	Reverse Transfer Capacitance		6.9	-		f=1.0MHz
Qg	Total Gate Charge		22			VDS=520V
Qgs	Gate-to-Source Charge		4.3		nC	ID=7A VGS=10V
Qgd	Gate-to-Drain("Miller") Charge		13			(Note:3,4)



### Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ls	Continuous Source Current			7.0	Α	Integral pn-diode
lsм	Maximum Pulsed Current			28.0	Α	in MOSFET
Vsd	Diode Forward Voltage			1.4	V	IS=7A,VGS=0V
trr	Reverse Recovery Time		300		nS	VGS=0V
Qrr	Reverse Recovery Charge		4.1		μC	IS=7A,di/dt=100A/µs

#### Notes:

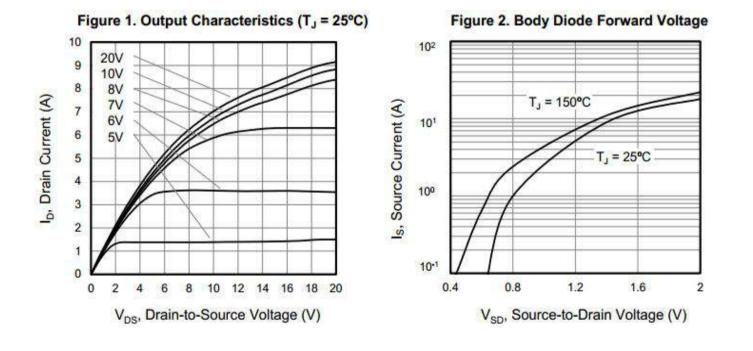
\*1.TJ=±25℃ to +150℃.

\*2.Repetitive rating; pulse width limited by maximum junction temperature.

\*3.Pulse width  $\leq$  300 µs; duty cycle  $\leq$  1%.

# Typical Feature curve $T_J = 2$

T<sub>J</sub> = 25°C, unless otherwise noted





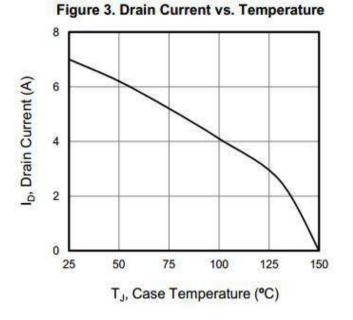
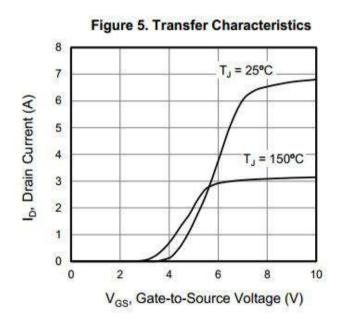
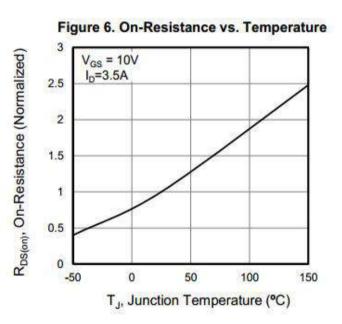


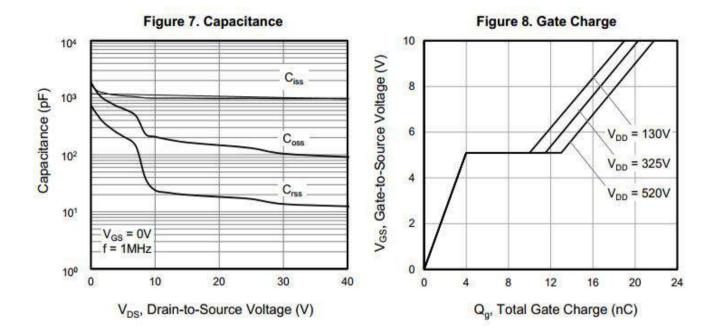
Figure 4. BV<sub>DSS</sub> Variation vs. Temperature 1.2  $V_{GS} = 0V$   $I_D = 250\mu A$  1.1 0.9 -50 -25 0 25 50 75 100 125 150T<sub>J</sub>, Junction Temperature (°C)











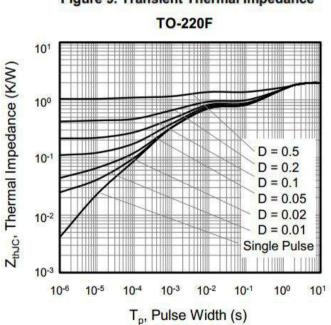


Figure 9. Transient Thermal Impedance



# **Test Circuits and Waveforms**

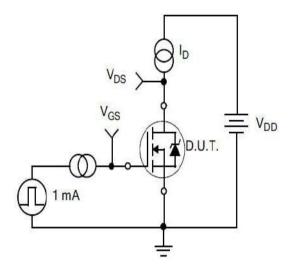


Figure10. Gate Charge Test Circuit

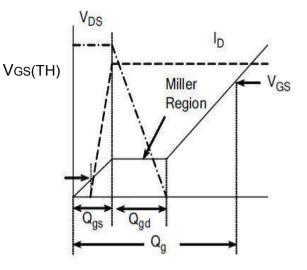


Figure11. Gate Charge Waveform

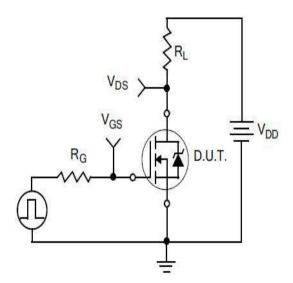


Figure12. Resistive Switching Test Circuit

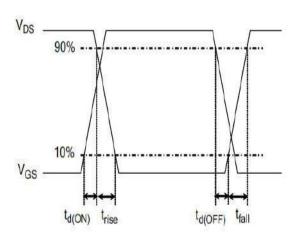
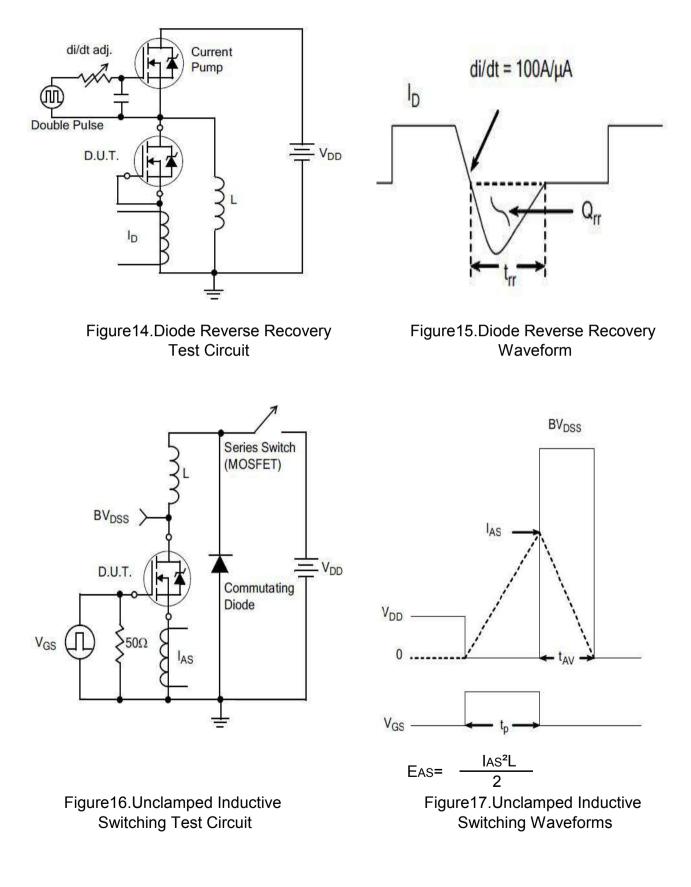


Figure13. Resistive Switching Waveforms



# **Test Circuits and Waveforms**



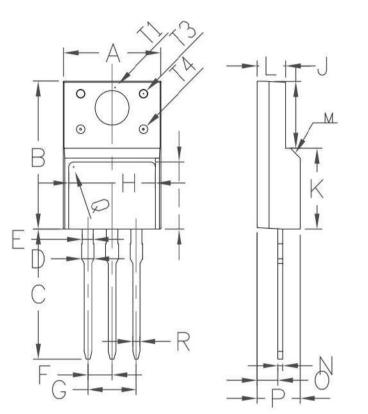


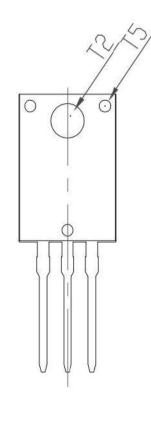
# RS7N65F

# Package outline drawing



Unit: mm





Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
С	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
Н	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8.99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
0	2.15	2.35	2,55
Р	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3.45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83



#### **Disclaimers:**

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights,nor the rights of others.Reproduction of information in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

#### Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

1.Life support devices or systems are devices or systems which:

a.are intended for surgical implant into the human body,

b.support or sustain life,

c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.