



#### 700V N Channel MOSFET

## **Applications:**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

# Features:

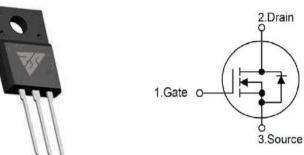
- •improved dv/dt capability •100% avalanche tested
- Fast switching
- •RoHS Compliant

### **Ordering Information**

Part Number	Package	Marking
RS6N70F	TO-220F	RS6N70F

Lead Free Package and Finish

lo	RDS(ON)(Typ.)	VDSS
6A	1.3Ω	700V



Not to Scale

# Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS6N70F	Units
VDSS	Drain-to-Source Voltage (Note*1)	700	V
ID	Continuous Drain Current	6	A
ldм	Pulsed Drain Current (Note*2)	24	
PD	Power Dissipation(Tc=25 °C)	63	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy IAS=6A VDD=50V RG=25Ω TJ=25℃	198	mJ
IAR	Avalanche Current	4.5	А
EAR	Repetitive Avalanche Engergy	40	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	300 260	$^{\circ}$
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage	-55 to 150	
	Temperature Range		

<sup>\*</sup>Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

#### **Thermal Resistance**

Symbol	Parameter	RS6N70F	Units	Test Conditions
Rejc	Junction-to-Case	1.98		Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150 ℃.
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.



# OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	700			٧	Vgs=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1.0	μΑ	VDS=700V,VGS=0V
Igss	Gate-to-Source Forward Leakage			100	nΛ	Vgs=+30V Vps=0V
1633	Gate-to-Source Reverse Leakage			-100	nA	Vgs=-30V Vds=0V

# ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		1.3	1.6	Ω	Vgs=10V,lp=3.0A
Vgs(TH)	Gate Threshold Voltage	3.0		4.0	V	Vgs=Vds,Id=250µA

# Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		15			VDS=350V
trise	Rise Time		18		no	ID=6A
td(OFF)	Turn-OFF Delay Time		80		ns	Rg=25Ω
tfall	Fall Time		35			

# **Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		891			Vgs=0V
Coss	Output Capacitance		110		pF	VDS=25V
Crss	Reverse Transfer Capacitance		14			f=1.0MHz
Qg	Total Gate Charge		22			Vps=560V
Qgs	Gate-to-Source Charge		4.3		nC	ID=6A
Qgd	Gate-to-Drain("Miller") Charge		13			VGS=10V

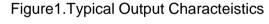


#### **Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current			6	Α	Integral pn-diode
Ism	Maximum Pulsed Current			24	Α	in MOSFET
Vsd	Diode Forward Voltage			1.4	V	Is=6A,Vgs=0V Tj=25℃
trr	Reverse Recovery Time		300		nS	Vgs=0V
Qrr	Reverse Recovery Charge		4.1		μC	ls=6A,di/dt=100A/µs

# Notes:

# Typical Feature curve $T_J=25^{\circ}C$ , unless otherwise noted



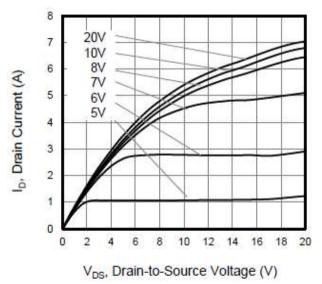
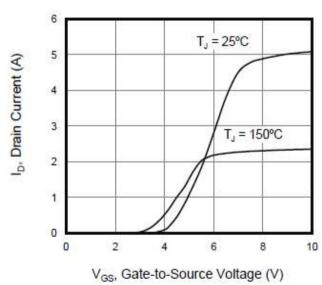


Figure 2. Typical Transfer Characteristics



Copyright Reasunos

http://www.reasunos.com

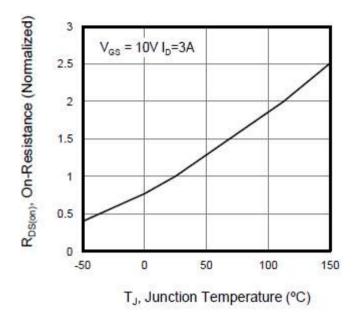
REV:A0 Apr.2018

<sup>\*1.</sup>TJ=±25°C to +150°C.

<sup>\*2.</sup>Repetitive rating; pulse width limited by maximum junction temperature.

<sup>\*3.</sup>Pulse width≤300µs;duty cycle ≤1%.

Figuer3.Typical ON-Resistance vs Temperature



Figuer4.Typical Body Diode Transfer Characteristics

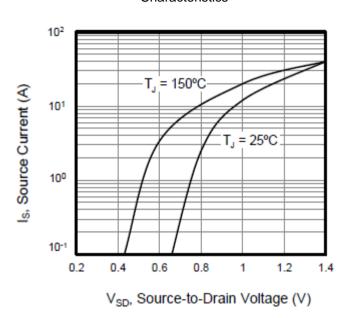


Figure 5. Typical Temperature vs Drain Current

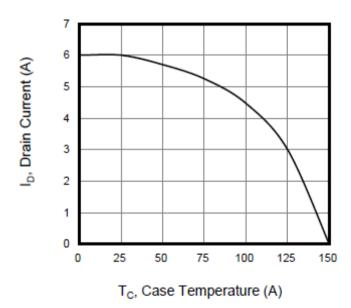


Figure6.Typical Temperature vs BVdss Variation

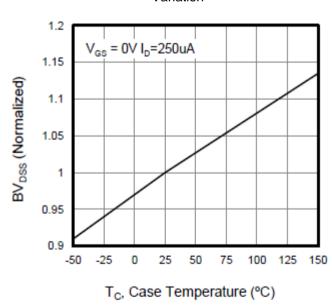


Figure 7. Typical Capacitance vs Drain-to-Source Voltage

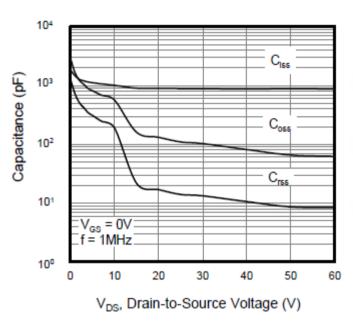


Figure8. Typical Gate Charge

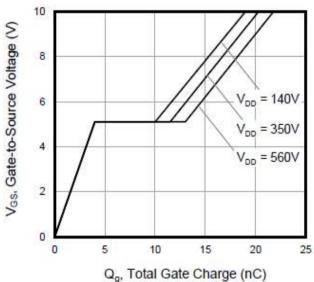
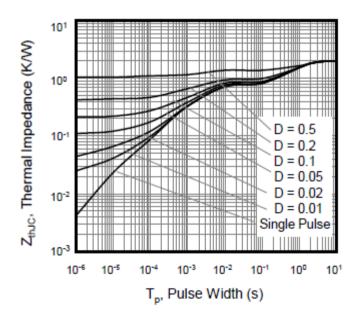


Figure9.Transient Thermal Impedance TO-220F



# **Test Circuits and Waveforms**

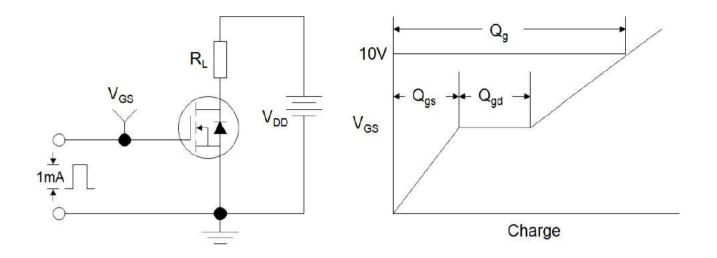


Figure 10.
Gate Charge Test Circuit and Waveform

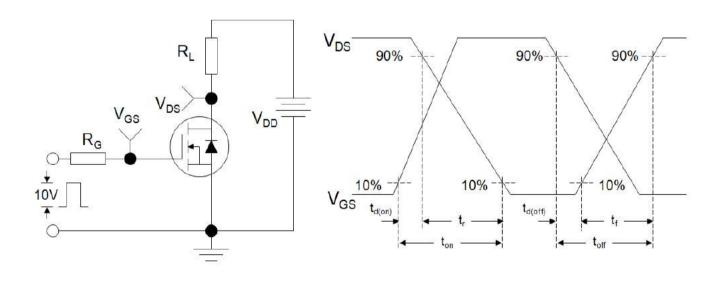


Figure 11.
Resistive Switching Test Circuit and Waveform



# **Test Circuits and Waveforms**

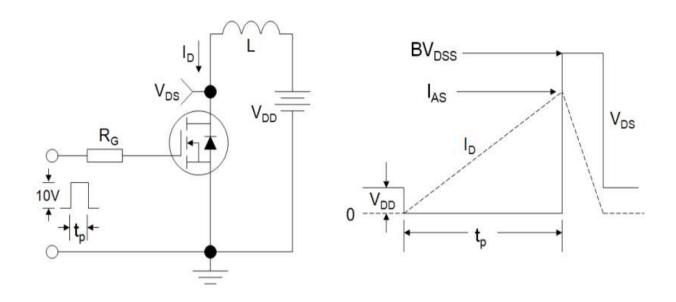


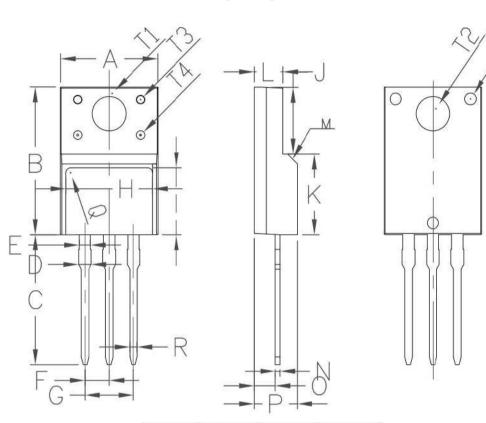
Figure 12. Unclamped Inductive Switching Test Circuit and Waveform



# Package outline drawing

TO-220F





Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
С	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
Н	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8. 99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
0	2.15	2.35	2.55
P	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3. 45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83



#### **Disclaimers:**

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights,nor the rights of others. Reproduction of information in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

#### **Life Support Policy:**

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

- 1.Life support devices or systems are devices or systems which:
  - a.are intended for surgical implant into the human body,
  - b.support or sustain life,
  - c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.