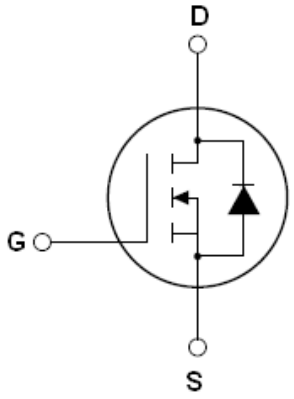
REASUNOS

N-Channel Super Junction Power MOSFET

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.



Schematic diagram

Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）

V_{DS}	650	V
$R_{DS(ON)Max.}$	840	mΩ
I_D	5.5	A

Package Marking And Ordering Information

Device	Device Package	Marking
RS65R950MD	TO-251	RS65R950MD
RS65R950D	TO-252	RS65R950D

TO-251

TO-252

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	650	V
Gate-Source Voltage (V_{DS}=0V) ,AC (f>1 Hz)	V_{GS}	±20	V
Continuous Drain Current at Tc=25°C	$I_{D\ (DC)}$	5.5	A
Continuous Drain Current at Tc=100°C	$I_{D\ (DC)}$	3	A
Pulsed drain current **(Note 1)**	$I_{DM\ (pluse)}$	16.5	A
Maximum Power Dissipation(Tc=25℃)	P_D	86	W
Single pulse avalanche energy **(Note2)**	E_{AS}	75	mJ

Parameter	Symbol	Value	Unit
Drain Source voltage slope, V_{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt， V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+150	°C

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	1.44	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	100	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=520V,V_{GS}=0V			10	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2		4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=2.5A		760	840	mΩ
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz		360		pF
Output Capacitance	C_{oss}			78		pF
Reverse Transfer Capacitance	C_{rss}			1.2		pF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=5A, V_{GS}=10V		11.9		nC
Gate-Source Charge	Q_{gs}			1.9		nC
Gate-Drain Charge	Q_{gd}			7.1		nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V,I_D=5A, R_G=5Ω,V_{GS}=10V		11		nS
Turn-on Rise Time	t_r			9		nS
Turn-Off Delay Time	$t_{d(off)}$			19		nS
Turn-Off Fall Time	t_f			5.2		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	T_C=25°C			5.5	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				16.5	A
Forward On Voltage	V_{SD}	Tj=25°C,I_{SD}=5A,V_{GS}=0V			1.2	V
Reverse Recovery Time	t_{rr}	Tj=25°C,I_F=5A,di/dt=100A/μs		230		nS
Reverse Recovery Charge	Q_{rr}			1.84		uC
Peak reverse recovery current	I_{rrm}			16		A

Notes: 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

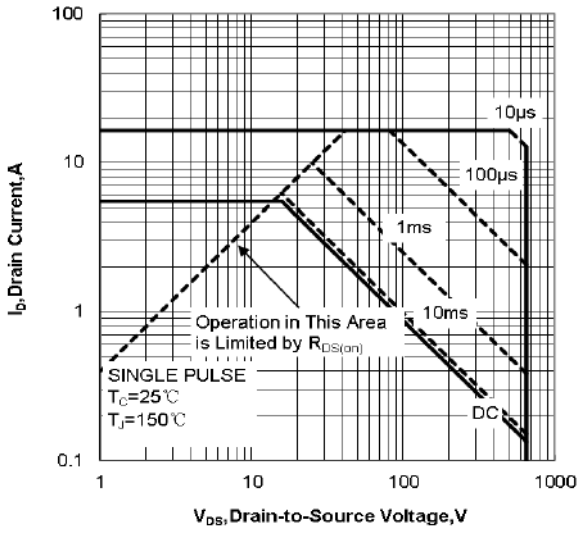


Figure.1MaximumForwardBiasSafeOperatingArea

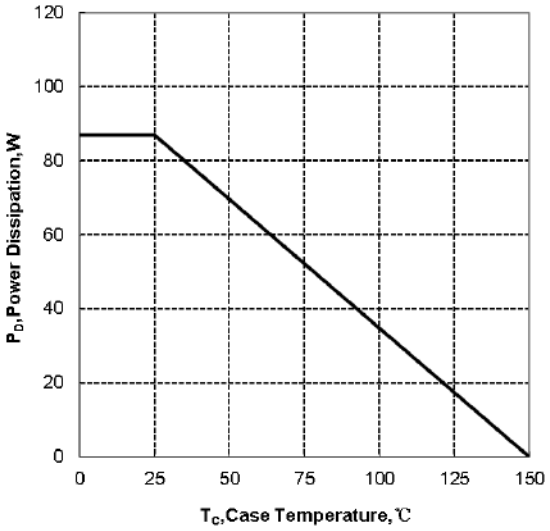


Figure.2MaximumPowerDissipationvsCaseTemperature

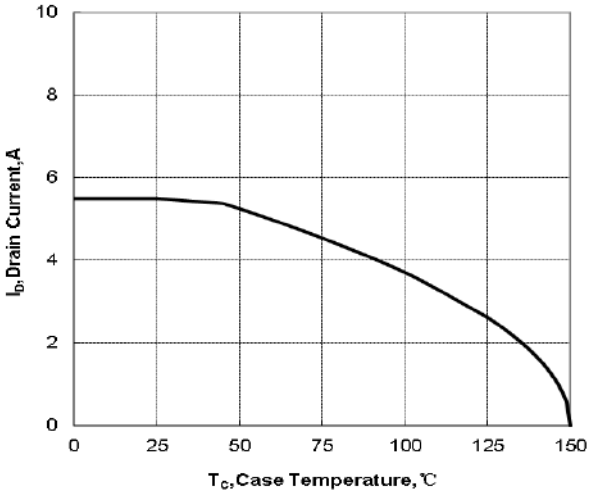


Figure.3MaximumContinuous DrainCurrentvsCaseTemperature

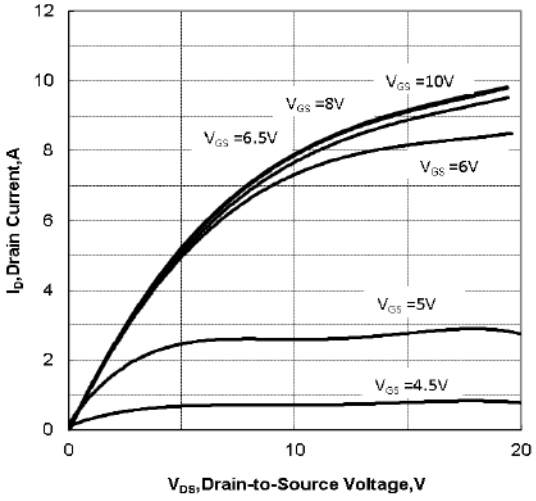


Figure.4TypicalOutputCharacteristics

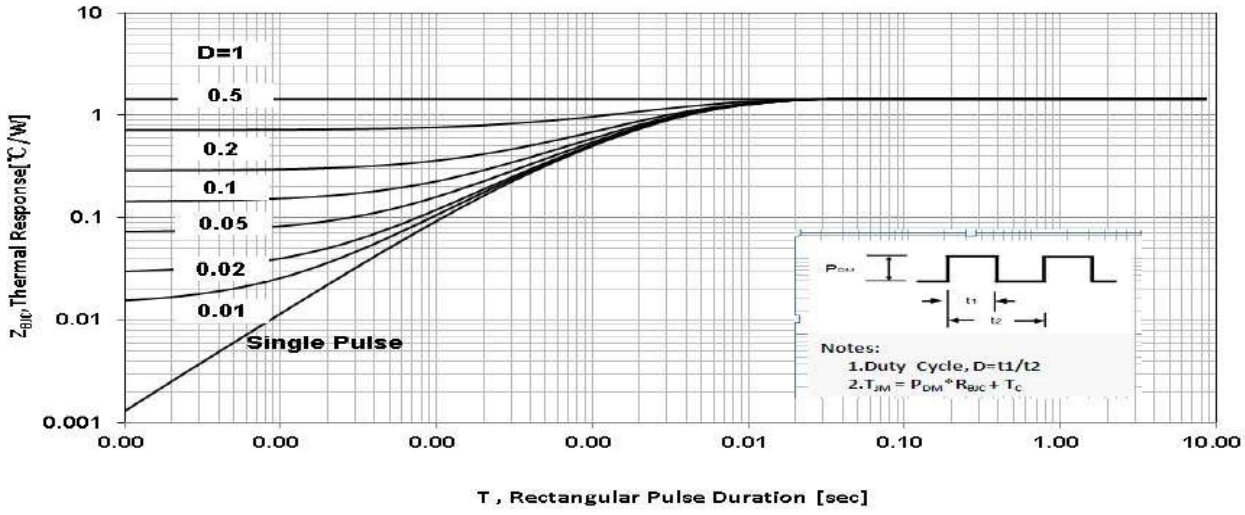


Figure.5Maximum Effective ThermalImpedance, JunctiontoCase

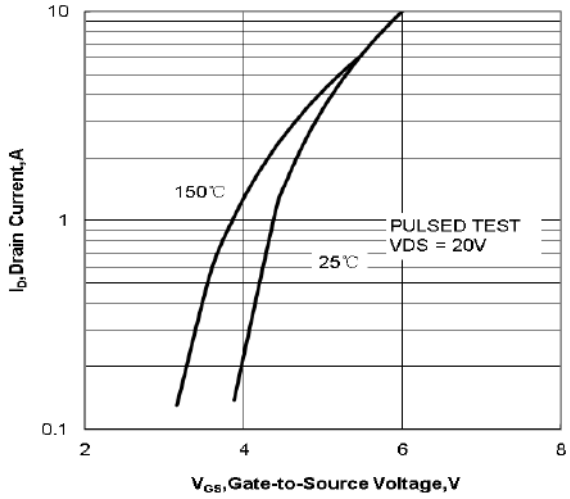


Figure.6TypicalTransferCharacteristics

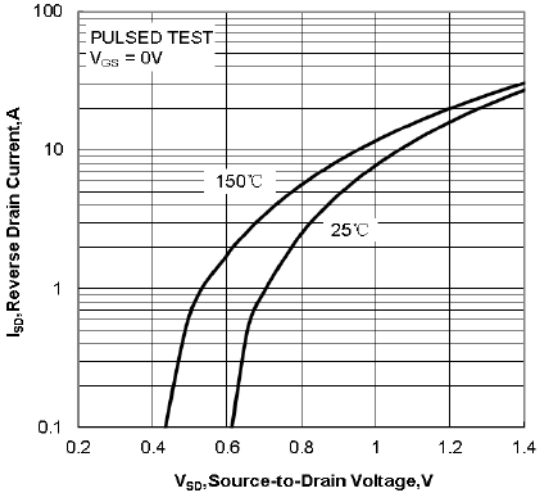


Figure.7TypicalBodyDiodeTransferCharacteristics

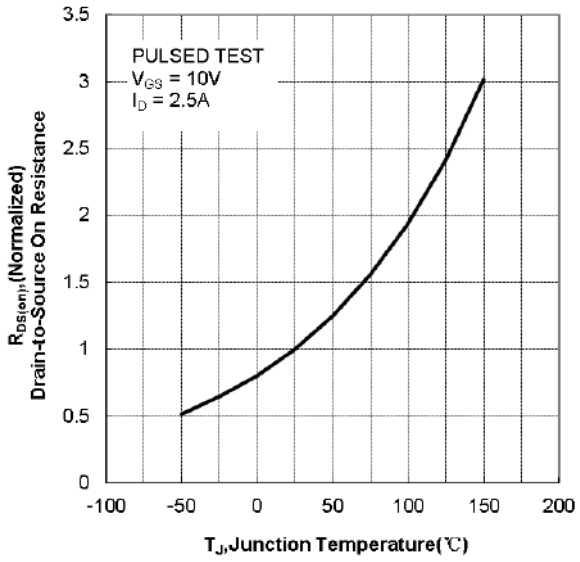


Figure.8TypicalDrainto Source ONResistance

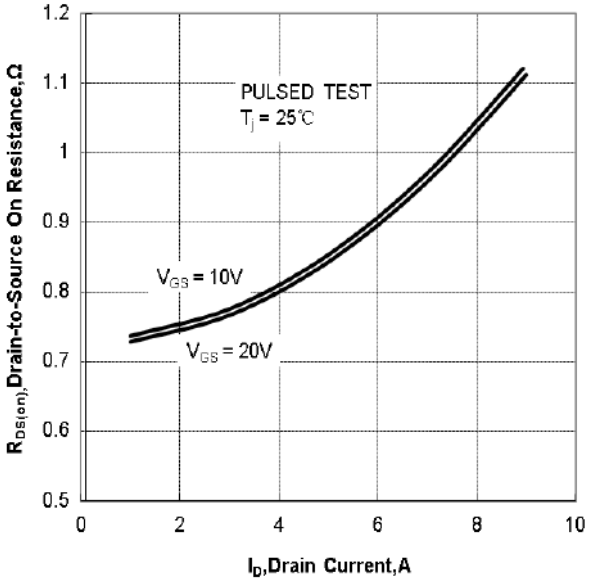


Figure.9Typical DriantoSource onResistance vs JunctionTemperature

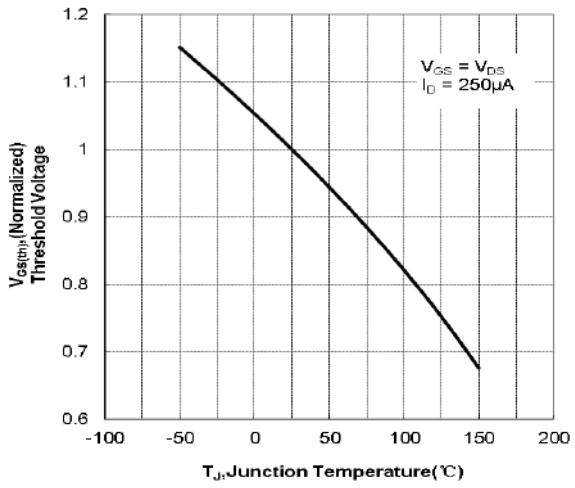


Figure.10TypicalThesholdVoltage vs JunctionTemperature

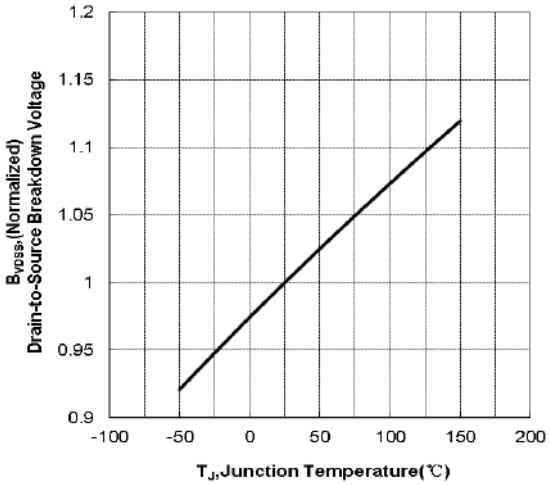


Figure11Typical BreakdownVoltage vs JunctionTemperature

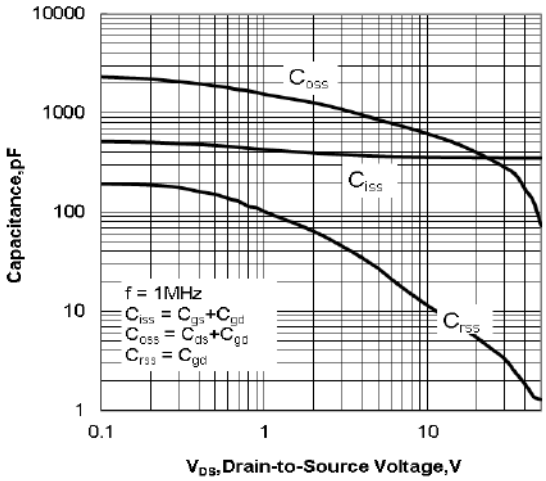


Figure.12TypicalCapacitance vsDrainto SourceVoltage

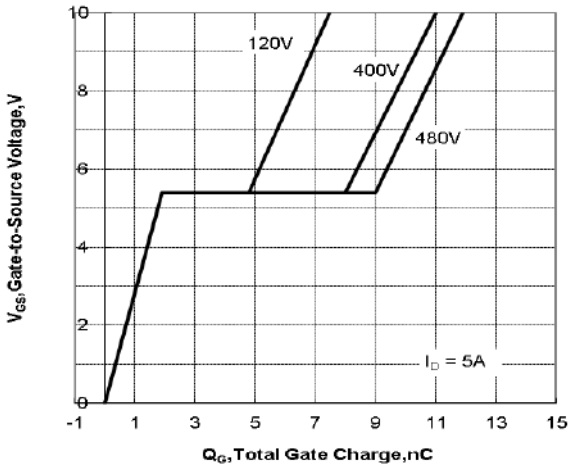


Figure.13TypicalGate ChargevsGate toSourceVoltage

Test circuit

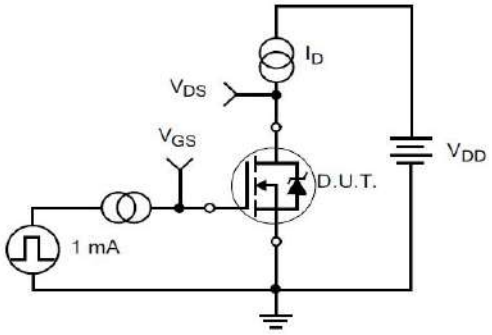


Figure 17. Gate Charge Test Circuit

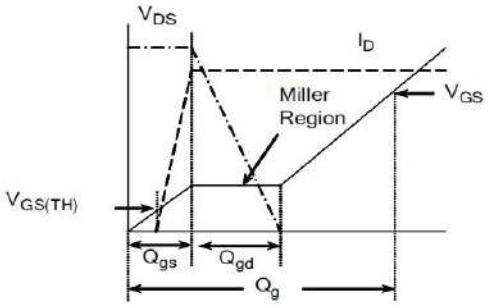


Figure 18. Gate Charge Waveform

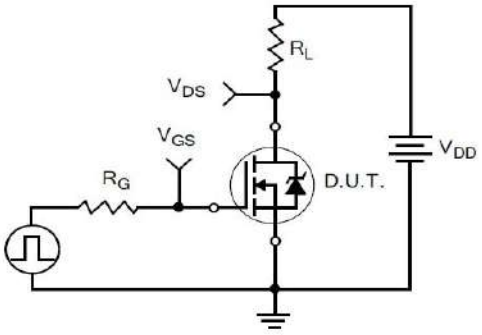


Figure 19. Resistive Switching Test Circuit

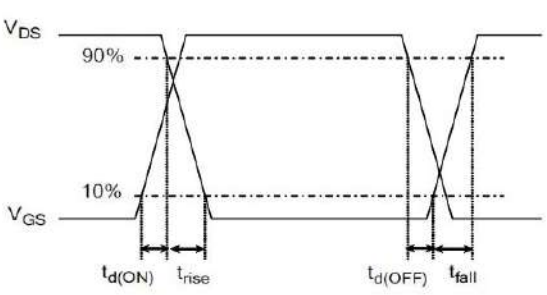


Figure 20. Resistive Switching Waveforms

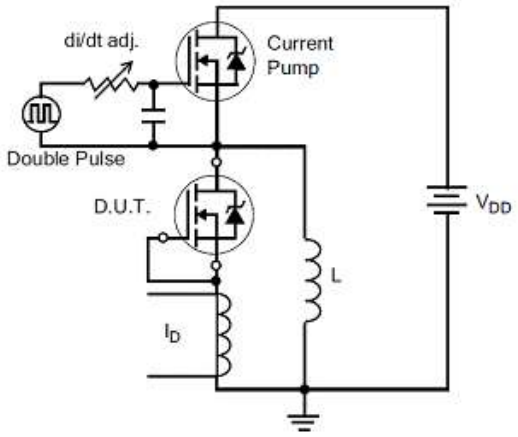


Figure 21. Diode Reverse Recovery Test Circuit

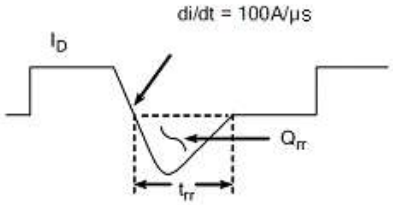


Figure 22. Diode Reverse Recovery Waveform

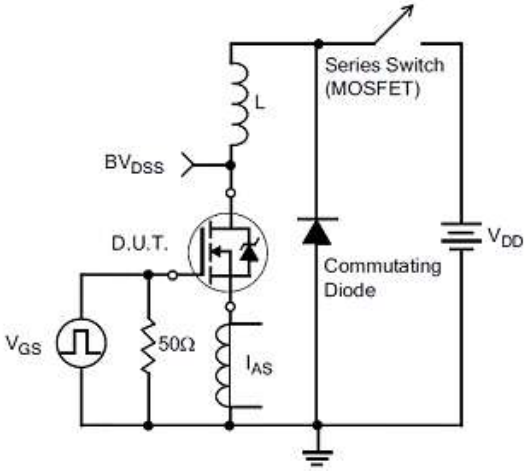


Figure 23. Unclamped Inductive Switching Test Circuit

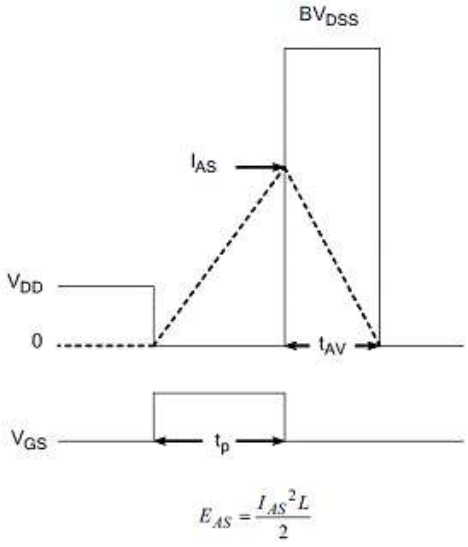
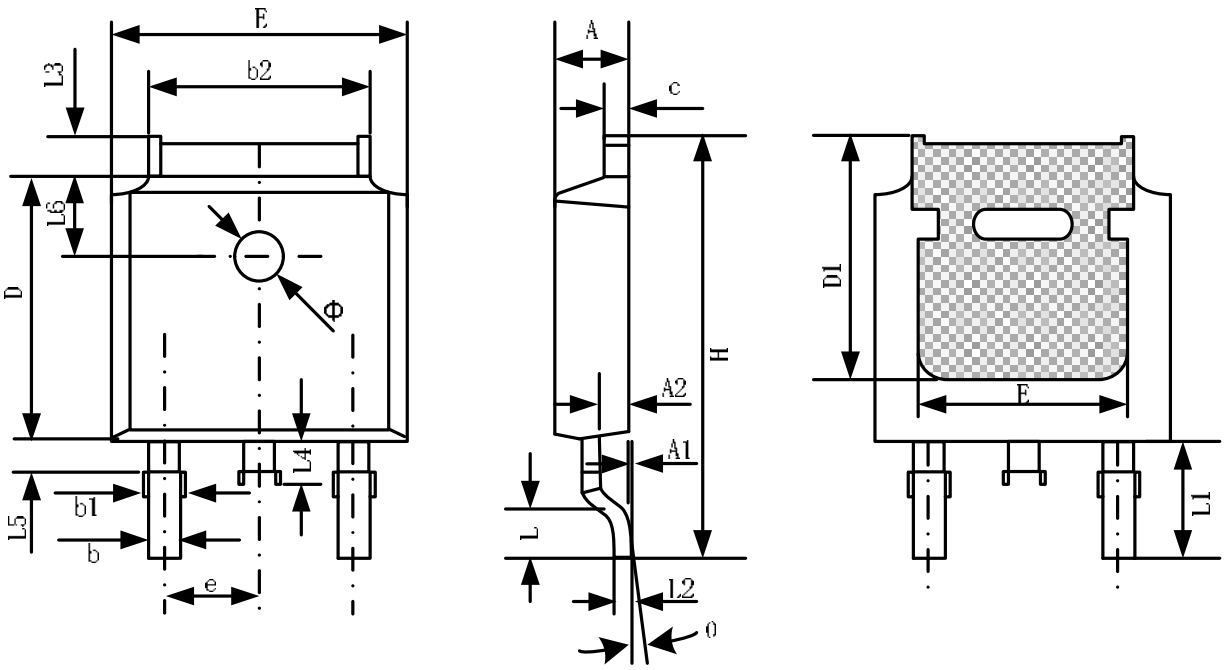


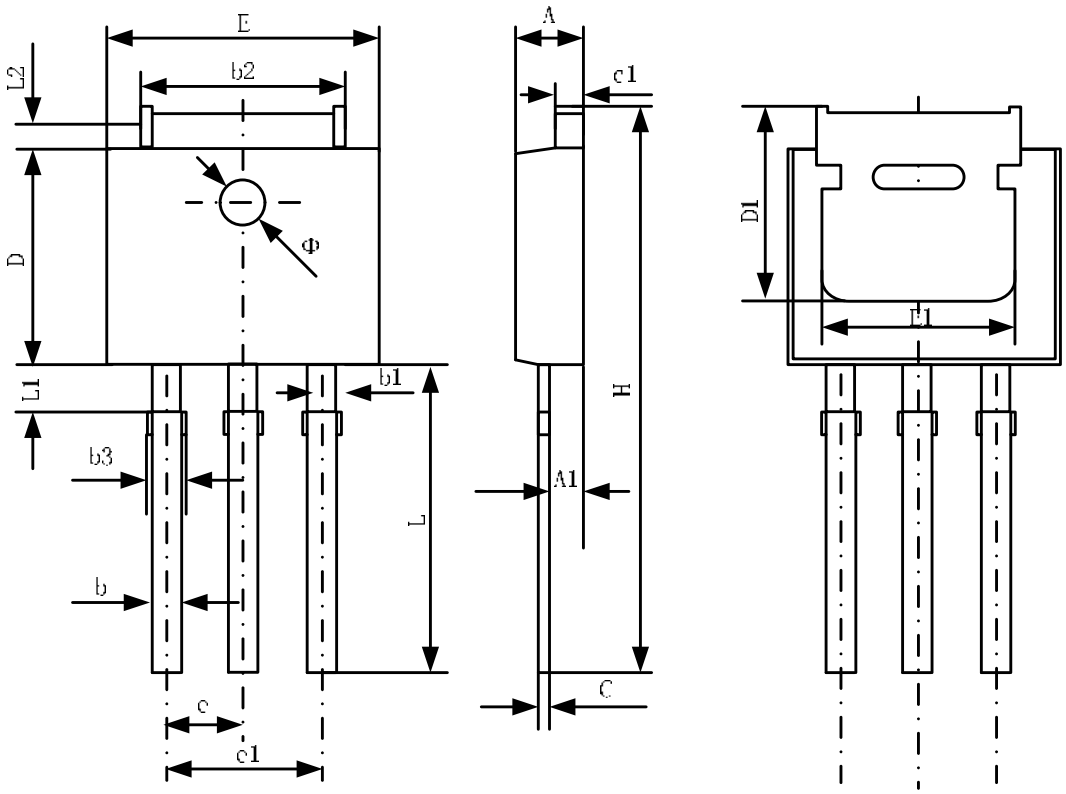
Figure 24. Unclamped Inductive Switching Waveforms

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
Φ	1.20	1.40	0.047	0.055
θ	0°	8°	0°	8°

TO-251 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.35	0.087	0.093
A1	0.90	1.10	0.035	0.043
b	0.56	0.69	0.022	0.027
b1	0.77	0.90	0.030	0.035
b2	5.23	5.43	0.206	0.214
b3		1.05	0.000	0.041
C	0.46	0.59	0.018	0.023
c1	0.46	0.59	0.018	0.023
D	6.00	6.20	0.236	0.244
D1	5.20		0.205	
E	6.50	6.70	0.256	0.264
E1	4.60	5.00	0.181	
e	2.24	2.34	0.088	0.092
e1	4.47	4.67	0.176	0.184
H	16.18	16.78	0.637	0.661
L	9.00	9.60	0.354	0.378
L1	0.95	1.35	0.037	0.053
L2	0.90	1.25	0.035	0.049

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b.support or sustain life,
c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.