Multi-Epi Super Junction MOSFETs

Lead Free Package and Finish

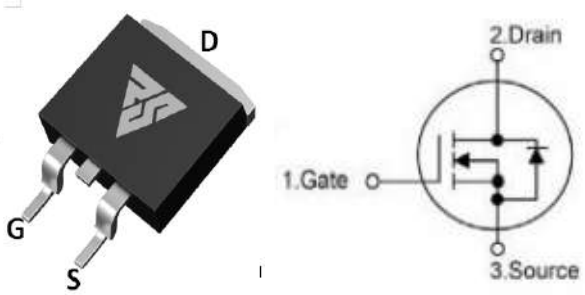
I_D	$R_{DS(ON)}$(Max.)	V_{DSS}
15A	280mΩ	650V

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- PFC stages for server & telecom
- Consumer

Features:

- New revolutionary high voltage technology
- Better RDS(on) in TO-252
- Ultra Low Gate Charge cause lower driving requirements
- Periodic avalanche rated
- Ultra low effective capacitances



Not to Scale

Ordering Information

Part Number	Package	Marking
RS65R280D	TO-252	RS65R280D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS65R280D	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current (TC = 25℃)	15	A
	Continuous Drain Current (TC = 100℃)	9	
I_{DM}	Pulsed Drain Current (Note*1)	45	
P_D	Power Dissipation(Tc=25℃)	80	W
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Engergy (Note*2)	310	mJ
I_{AR}	Avalanche Current (Note*1)	2.2	A
T_L	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds	300	℃
T_{PKG}	Package Body for 10 seconds	260	
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the"Absolute Maximum Ratings"Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS65R280D	Units	Test Conditions
RθJC	Junction-to-Case	0.93	℃/W	Drain lead soldered to water cooled heatsink ,PD Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	96		1 cubic foot chamber ,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650	--	--	V	VGS = 0V, ID = 250μA, TJ= 25℃
		--	650	--	V	VGS = 0V, ID = 250μA, TJ= 150℃
IDSS	Drain-to-Source Leakage Current	--	--	1.0	μA	VDS=650V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+30V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	240	280	mΩ	VGS=10V,ID=7.5A
VGS(TH)	Gate Threshold Voltage	2.5	--	4.5	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	20	--	ns	VDS=400V ID=7.5A RG=25Ω VGS=10V
trise	Rise Time	--	40	--		
td(OFF)	Turn-OFF Delay Time	--	95			
tfall	Fall Time	--	43			

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1126	--	pF	VGS=0V VDS=100V f=1.0MHz
Coss	Output Capacitance	--	41	--		
Crss	Reverse Transfer Capacitance	--	2.4	--		
Qg	Total Gate Charge	--	26	--	nC	VDS=520V ID=7.5A VGS=10V
Qgs	Gate-to-Source Charge	--	3.5	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	10.5	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	15	A	Integral pn-diode in MOSFET
ISM	Maximum Pulsed Current	--	--	45	A	
VSD	Diode Forward Voltage	--	0.85	1.4	V	IS=7.5A,VGS=0V Tj=25℃
trr	Reverse Recovery Time	--	405	--	nS	VR=400V,VGS=0V IS=7.5A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	4.0	--	μC	
Irrm	Peak Reverse Recovery Current	--	21	--	A	

Notes:

*1.Repetitive rating;pulse width limited by maximum junction temperature.
*2. Pulse width tp limited by Tj,max

Typical Feature curve T_J=25℃, unless otherwise noted

Figure 1. Output Characteristics

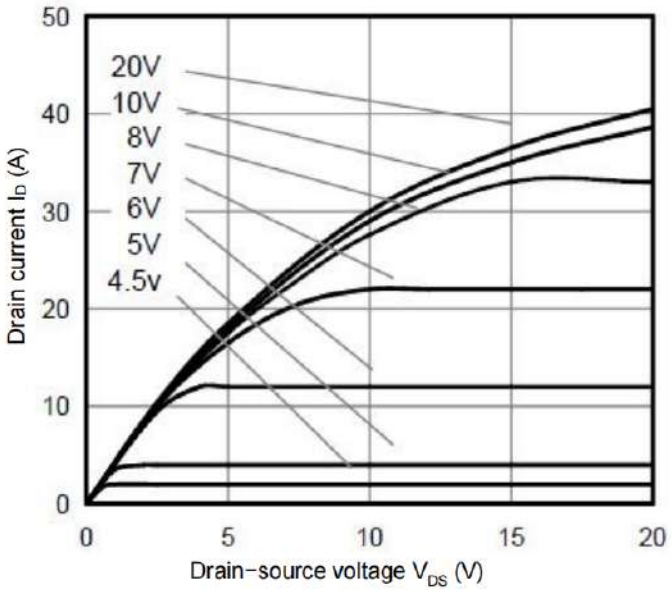


Figure 2. Transfer Characteristics

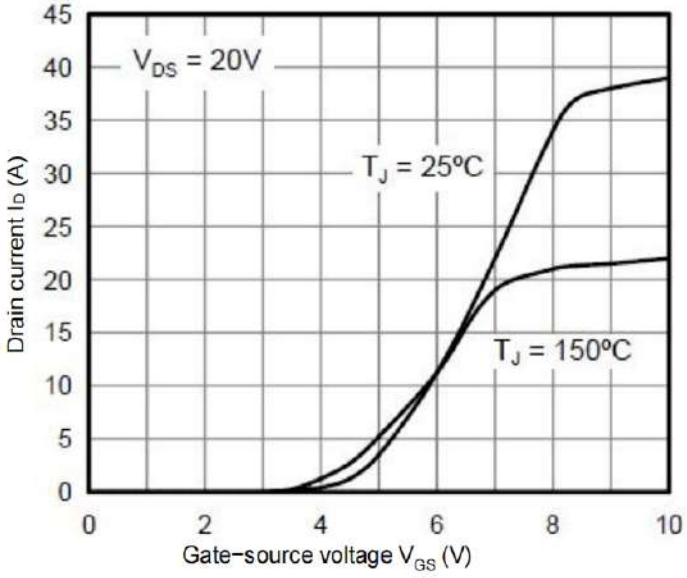


Figure 3. On-Resistance vs. Drain Current

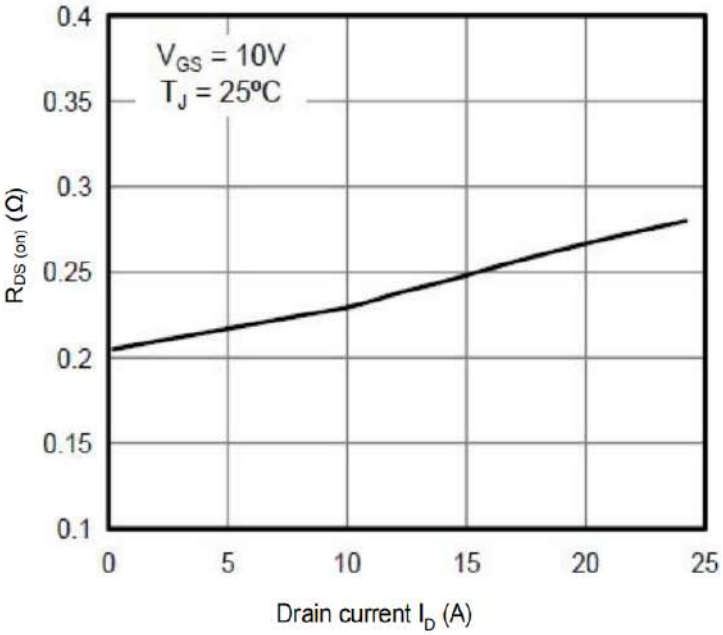


Figure 4. Capacitance Characteristics

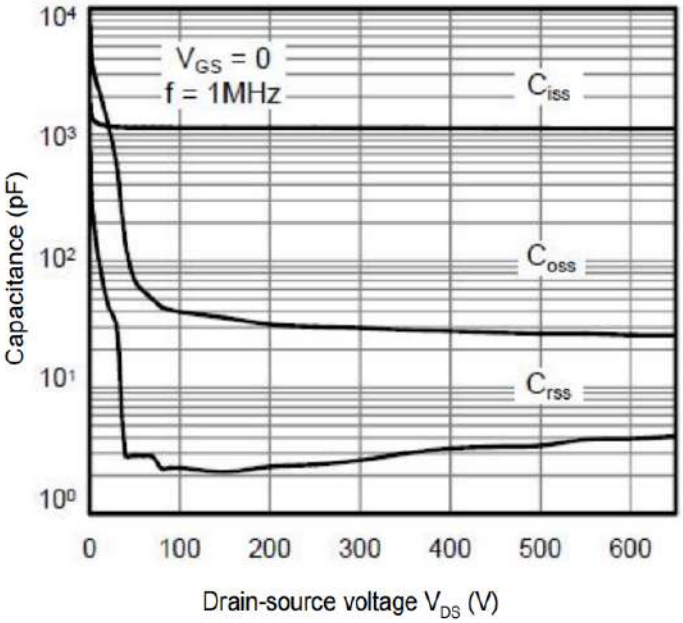


Figure 5. Gate Charge Characteristics

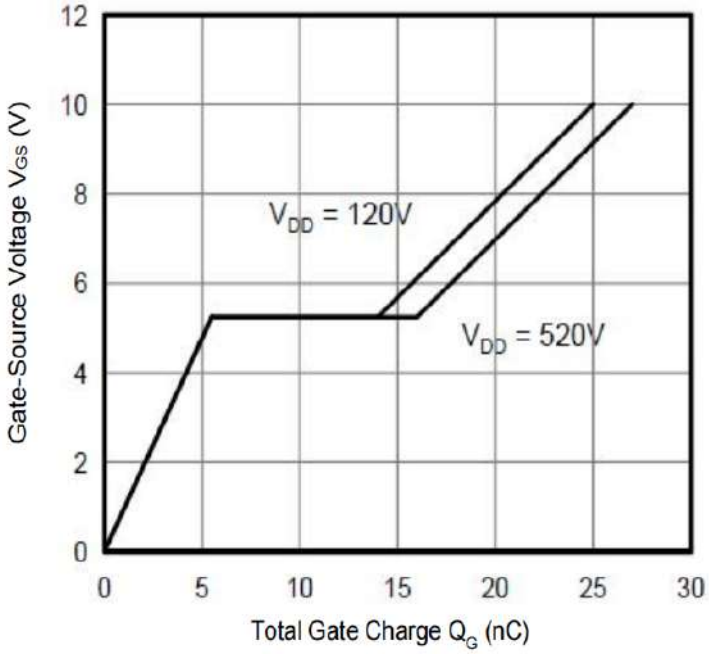


Figure 6. Body Diode Forward Voltage

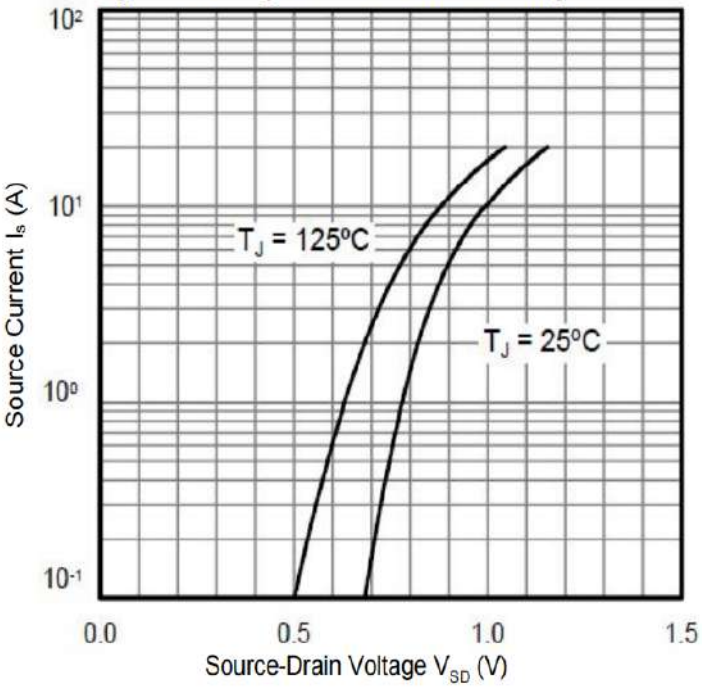


Figure 7. Breakdown Voltage vs. Temperature

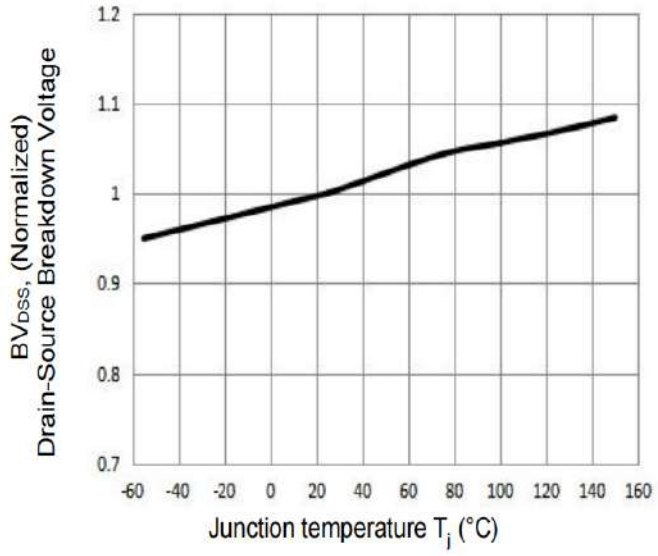


Figure 8. On-Resistance vs. Temperature

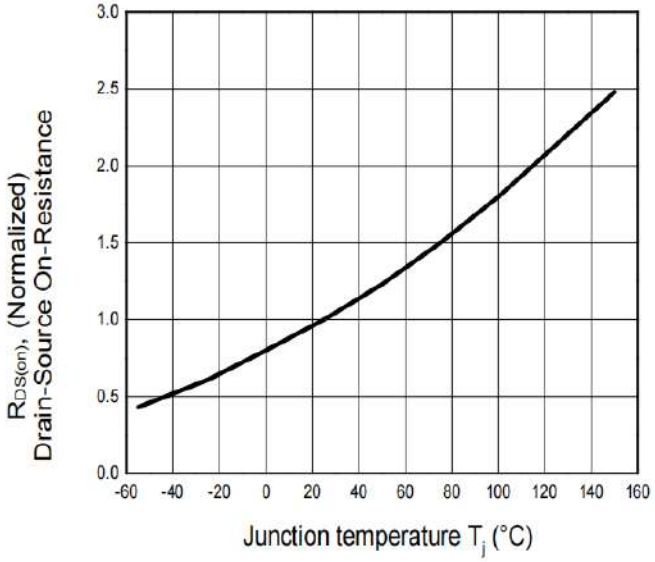
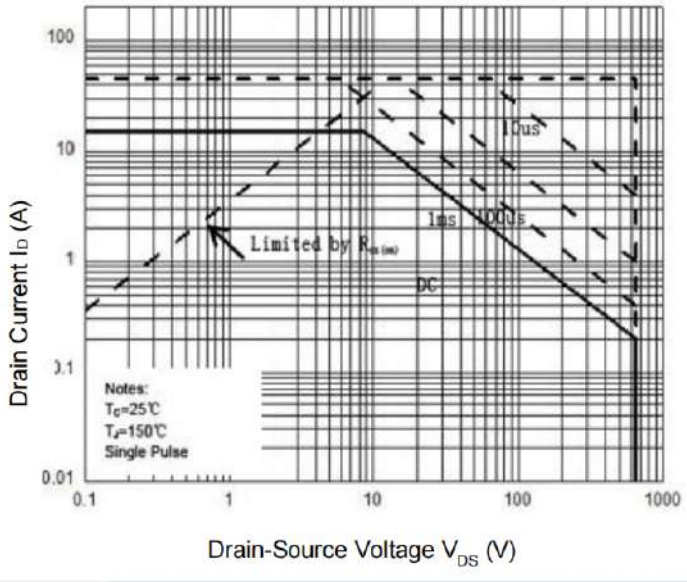


Figure 9. Maximum Safe Operating Area



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

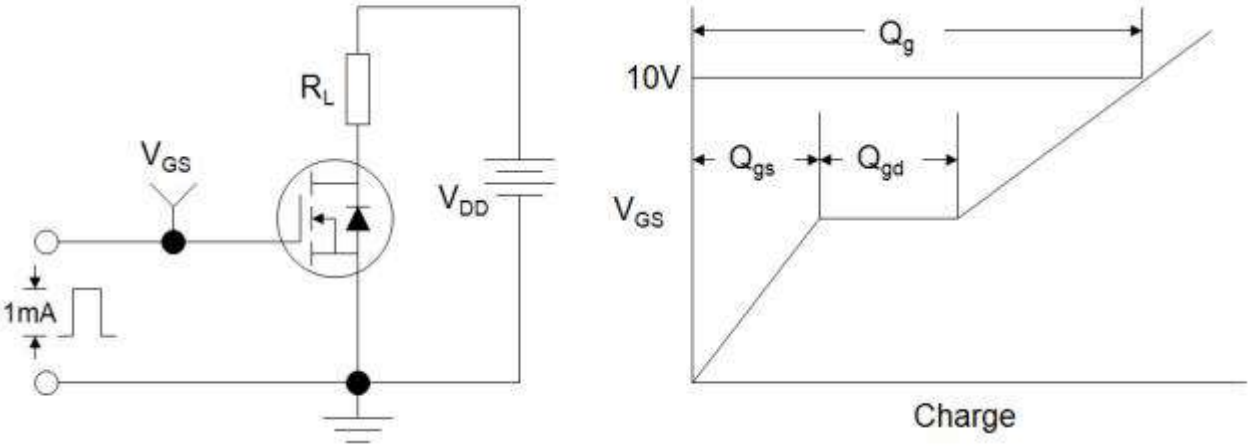


Figure B: Resistive Switching Test Circuit and Waveform

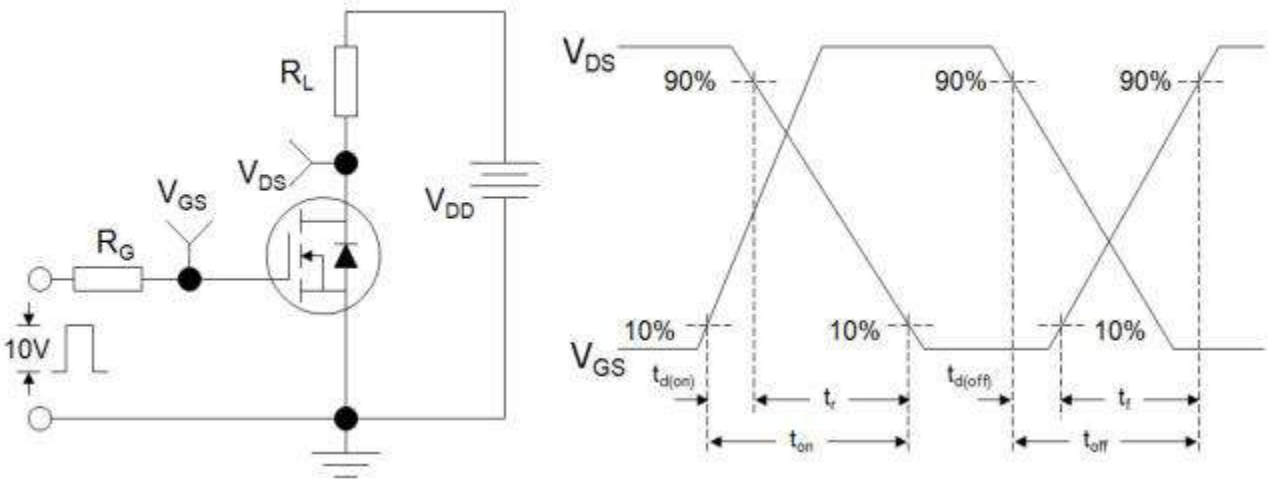
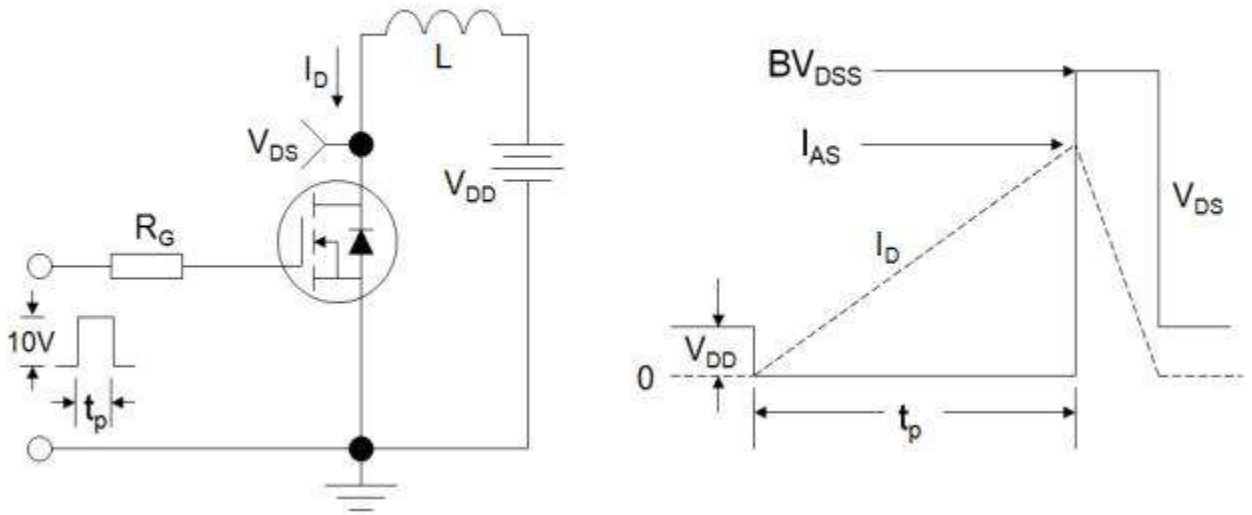
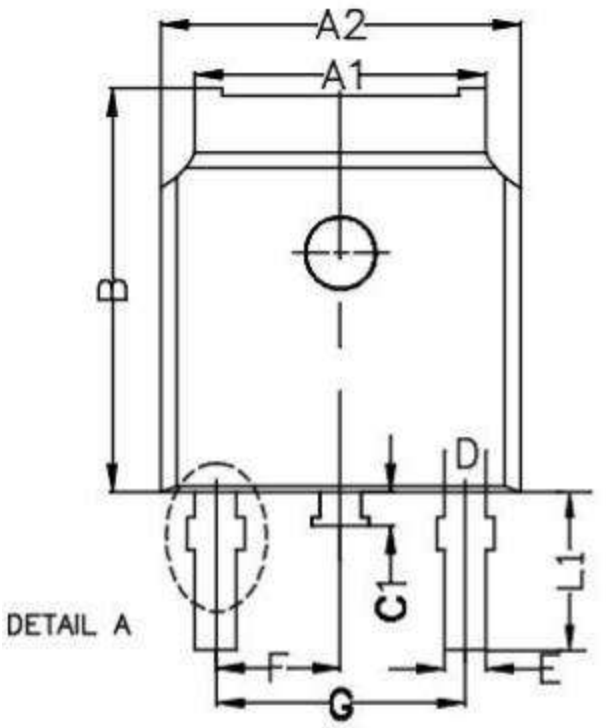


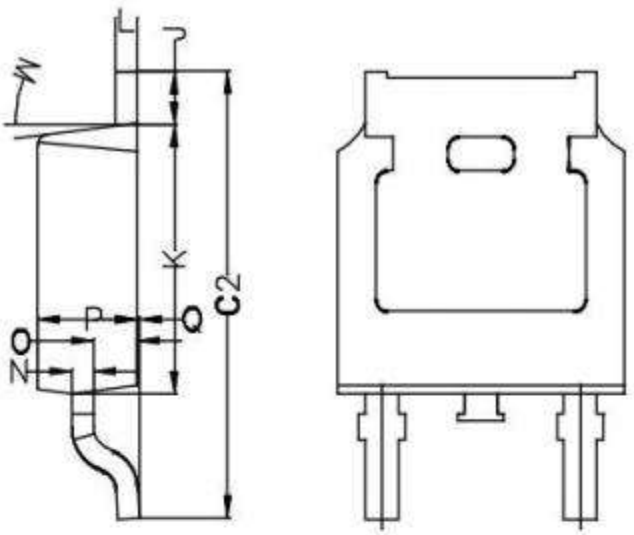
Figure C: Unclamped Inductive Switching Test Circuit and Waveform

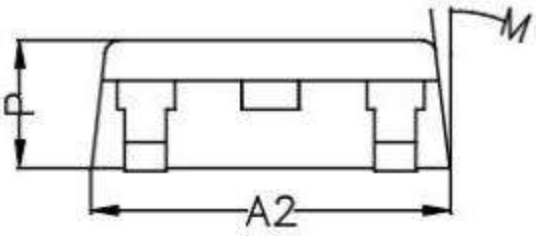


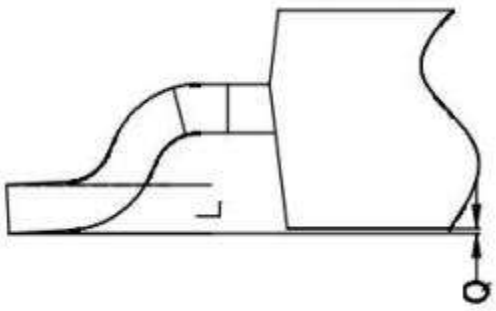
Package outline drawing

Unit:mm









Symbol	Min	Non	Max
A1	5.22	5.32	5.42
A2	6.55	6.60	6.65
B	7.05	7.10	7.15
C1	0.70	0.80	0.90
C2	9.70	9.90	10.10
D	1.00 REF.		
E	0.76 REF.		
F	2.286 REF.		
G	4.572 REF.		
J	0.95	1.00	1.05
K	6.05	6.10	6.15
L	0.508 REF.		
L1	2.65	2.80	2.95
M	7° REF.		
N	0.508 REF.		
O	0.96	1.01	1.06
P	2.25	2.30	2.35
Q	0.00	0.05	0.10

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