

RS60N50D

2.Drain

N Channel MOSFET

Applications:

- •PWM applications
- ·Load switch
- Power management

P6)

Lead Free Package and Finish

lD	Rds(ON)(Max.)	VDSS
50A	20mΩ	60V

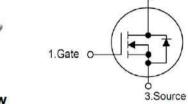
Features:

•VDS=60V; ID=50A

RDS(ON) < $20m\Omega$ @ VGS = 10V Rds(on) < $25m\Omega$ @ VGS = 4.5V

- •Ultra Low On-Resistance
- •High UIS and UIS 100% Test
- •RoHS Compliant





TO-252(DPAK) top view

Ordering Information

Part Number	Package	Marking
RS60N50D	TO-252	RS60N50D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS60N50D	Units
VDSS	Drain-to-Source Voltage	60	V
ID	Continuous Drain Current (Tc=25℃)	50	
ID	Continuous Drain Current Tc=100℃	35	Α
IDM	Pulsed Drain Current (Note*1)	200	1
PD	Power Dissipation (Tc=25℃)	89	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy (Note*2)	85	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	$^{\circ}$ C
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 175	

^{*}Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS60N50D	Units	Test Conditions
RθJC	Junction-to-Case	1.8	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +175℃.

Copyright Reasunos http://www.reasunos.com REV:A0 JULY 2021 Page 1 of 8



RS60N50D

OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	60			V	VGS=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1	μΑ	VDS=60V,VGS=0V
IGSS	Gate-to-Source Forward Leakage			100	nΛ	VGS=+20V VDS=0V
1633	Gate-to-Source Reverse Leakage			-100	nA	VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Ctatic Drain to Course On Desigtence (Neta*2)		14.0	20.0	mΩ	VGS=10V,ID=30A
KD3(0II)	Static Drain-to-Source On-Resistance (Note*3)		17.0	25.0	mΩ	VGS=4.5V,ID=30A
VGS(TH)	Gate Threshold Voltage	1.2	1.6	2.5	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		7.4			VDS=30V
trise	Rise Time		5.1		"C	VGS=10V
td(OFF)	Turn-OFF Delay Time		28.2		nS	RL=6.7 RG=3Ω
tfall	Fall Time		5.5			1/0-27

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		2050			VGS=0V
Coss	Output Capacitance		158		pF	VDS=30
Crss	Reverse Transfer Capacitance		120			Vf=1.0MHz
Qg	Total Gate Charge		50			VDS=30V
Qgs	Gate-to-Source Charge		6		nC	ID=20A
Qgd	Gate-to-Drain("Miller") Charge		15			VGS=10V

Copyright Reasunos http://www.reasunos.com REV:A0 JULY 2021 Page 2 of 8



RS60N50D

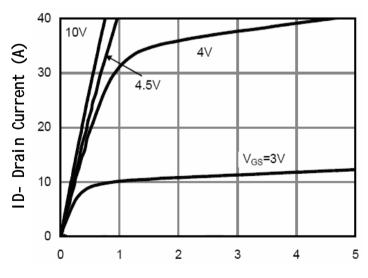
Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ISD	Source-Drain Current(Body Diode)		-	50	Α	
ISDM	Pulsed Source-Drain Current(Body Diode)			200		Maximum Pulsed Drain to Source Diode Forward Current
Vsd	Diode Forward Voltage			1.2	V	IS=20A,VGS=0V
trr	Reverse Recovery Time		28		nS	VGS=0V
Qrr	Reverse Recovery Charge		40		nC	IF=120A,di/dt=100A/μs

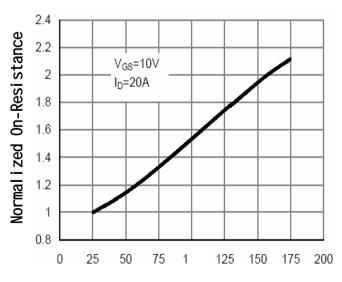
Notes:

- *1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- *2. EAS condition: TJ=25 $^{\circ}$ C, VDD=30V, VG=10V, L=0.5mH, RG=25 Ω
- *3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%

Typical Electrical and Thermal Characteristics (Curves)



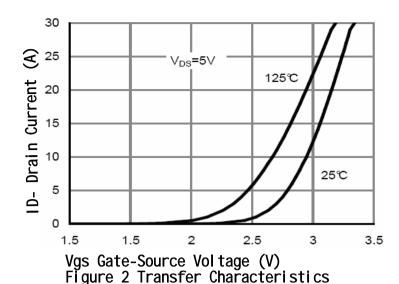
Vds Drain-Source Voltage (V) Figure 1 Output Characteristics

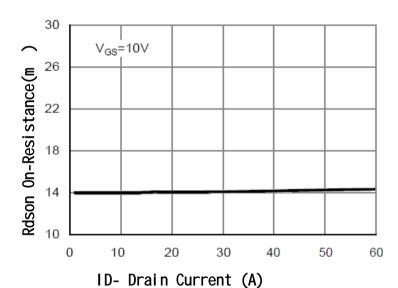


TJ-Junction Temperature()
Figure 4 Rdson-Junction Temperature

Copyright Reasunos http://www.reasunos.com REV:A0 JULY 2021 Page 3 of 8

RS60N50D





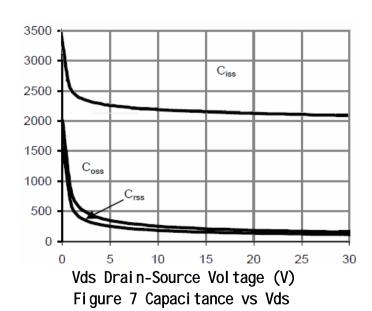
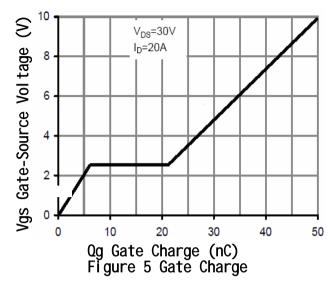
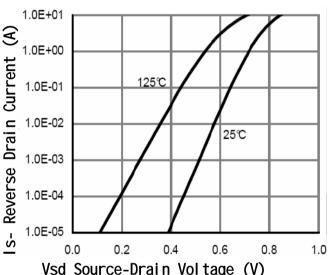
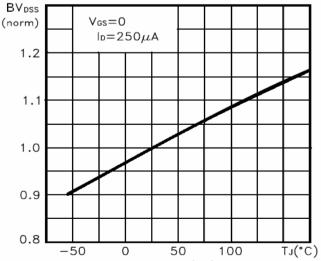


Figure 3 Rdson- Drain Current

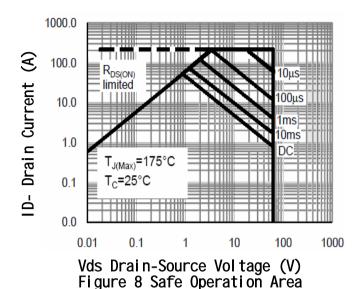


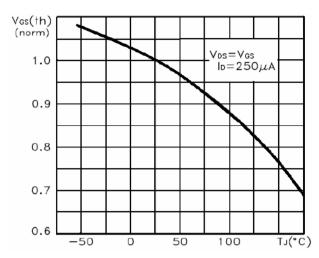


Vsd Source-Drain Voltage (V) Figure 6 Source- Drain Diode Forward

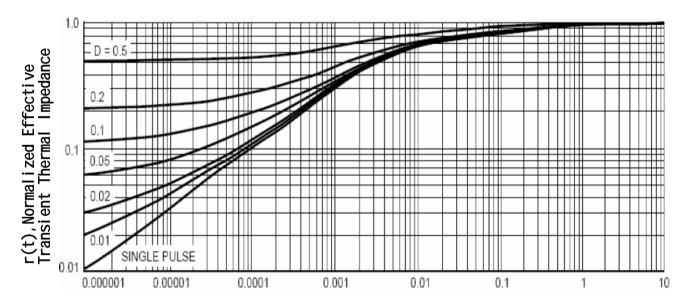


TJ-Junction Temperature()
Figure 10 VGS(th) vs Junction Temperature





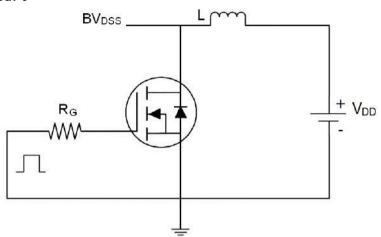
TJ-Junction Temperature()
Figure 10 VGS(th) vs Junction Temperature



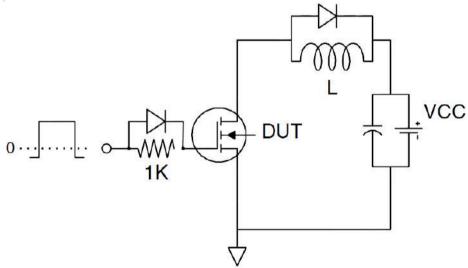
Square Wave Pluse Duration (sec) Figure 11 Normalized Maximum Transient Thermal Impedance

RS60N50D

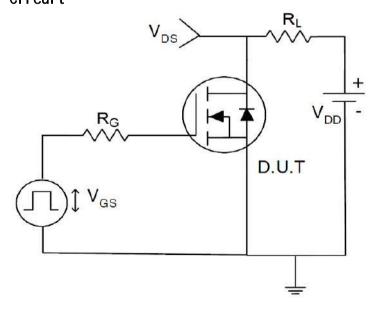
Test Circuit 1) EAS test Circuit



2) Gate charge test Circuit

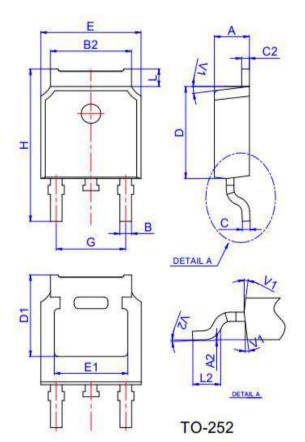


3) Switch Time Test Circuit





Package outline drawing



	Dimensions								
Ref.		Millimete	ers	Inches					
	Min.	Тур.	Max.	Min.	Typ.	Max			
A	2.10		2.50	0.083		0.098			
A2	0		0.10	0		0.004			
В	0.66		0.86	0.026		0.034			
B2	5.18		5.48	0.202		0.216			
С	0.40		0.60	0.016		0.024			
C2	0.44		0.58	0.017		0.023			
D	5.90		6.30	0.232		0.248			
D1		5.30REF	ii i	10	.209RE	209REF			
E	6.40		6.80	0.252		0.268			
E1	4.63			0.182					
G	4.47		4.67	0.176		0.184			
н	9.50	8	10.70	0.374		0.421			
L	1.09	8	1.21	0.043	č	0.048			
L2	1.35		1.65	0.053		0.065			
V1		7°			7°				
V2	0°		6°	0°		6°			

RS60N50D

Disclaimers:

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using Reasunos's components. To minimize risk, customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights,nor the rights of others.Reproduction of information in Reasunos's data sheets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

- 1.Life support devices or systems are devices or systems which:
 - a.are intended for surgical implant into the human body,
 - b.support or sustain life,
 - c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.
- 2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Copyright Reasunos http://www.reasunos.com REV:A0 JULY 2021 Page 8 of 8