N Channel MOSFET

Lead Free Package and Finish

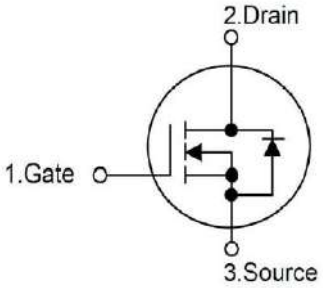
Applications:

- •Adapter & Charger
- •AC-DC Switching Power Supply
- •LED driving power
- •PC Power Supply

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
5A	1.9Ω	650V

Features:

- •100% avalanche tested
- •Ultra low gate Charge(typical 14nC)
- •Low Cress(typical 5.4pF)
- •Fast switching capability
- •RoHS Compliant



Not to Scale

Ordering Information

Part Number	Package	Marking
RS5N65D	TO-252	RS5N65D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS5N65D	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	650	V
I_D	Continuous Drain Current	5	A
I_D@ 100 ℃	Continuous Drain Current	3.2	
I_{DM}	Pulsed Drain Current (Note*2)	20	
PD	Power Dissipation	38	W
	Derating Factor above 25℃	0.3	W/℃
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=29mH IAS=5A VDD=50V RG=25Ω TJ=25℃	232	mJ
EAR	Repetitve Pulse Avalanche Engergy (pulse width limied by maximum junction temperature)	15	mJ
TL	Maximum Temperature for Soldering	300	℃
TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS5N65D	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.56	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	110		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	650	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=650V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	--	1.90	2.40	Ω	V_{GS}=10V,I_D=2.5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA
Gfs	Forward Transconductance		2.5		S	V_{DS}=50V,I_D=2.5A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	15	--	nS	V_{DS}=325V I_D=5A R_G=10Ω (Note:3,4)
t_{rise}	Rise Time	--	30	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	20	--		
t_{fall}	Fall Time	--	14	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	570	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	56	--		
C_{rss}	Reverse Transfer Capacitance	--	5.4	--		
Q_g	Total Gate Charge	--	14	--	nC	V_{DS}=520V I_D=5A V_{GS}=10V (Note:3,4)
Q_{gs}	Gate-to-Source Charge	--	3.8	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	7.5	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	5	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	20	A	
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=5A,V_{GS}=0V
trr	Reverse Recovery Time	--	513	--	nS	V_{GS}=0V I_S=5A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	2.6	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤2%.
*4.Basically not affected by temperature.

Typical Feature curve

Figure1.TypicalOutput Characteistics

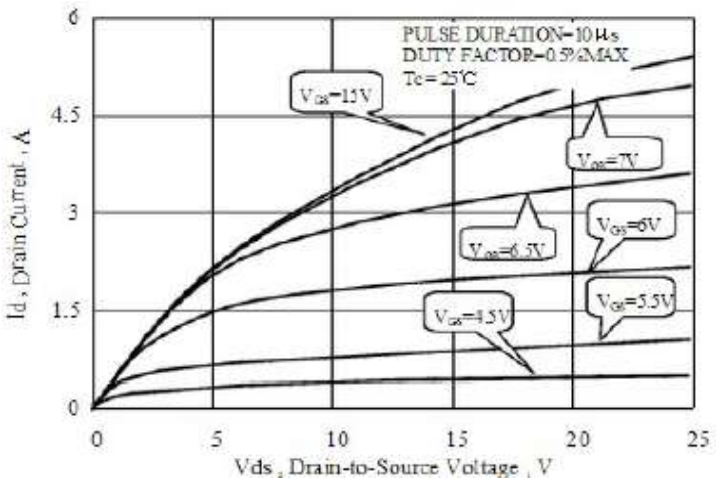
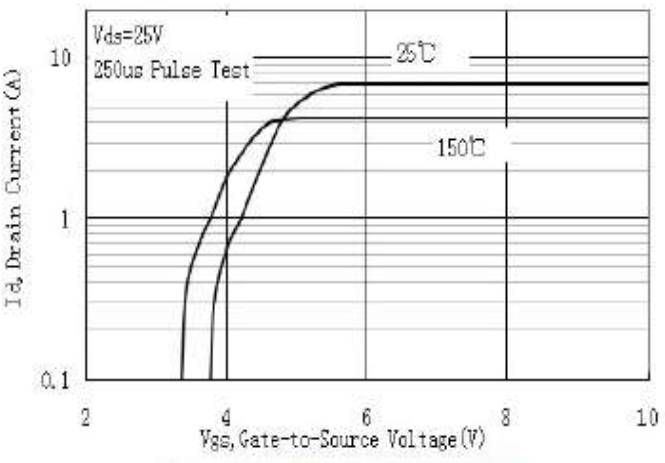
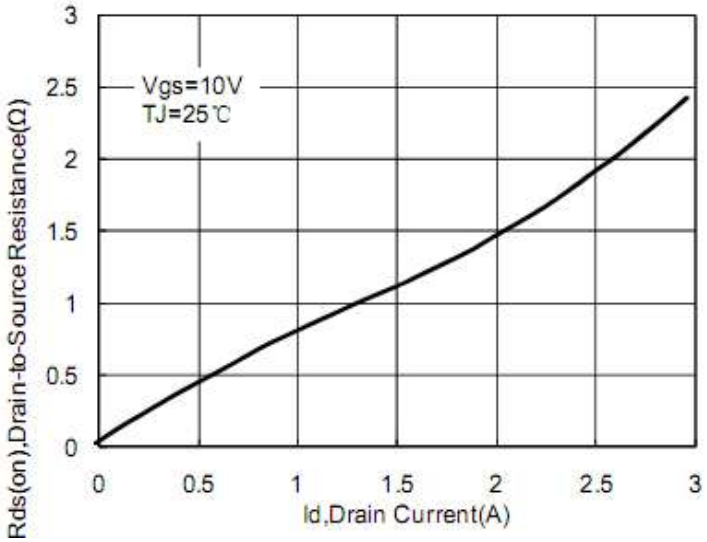


Figure2.Typical Transfer Characteristics



Figuer3.Typical ON Resistance vs Drain Current



Figuer4.Typical Body Diode Transfer Characteristics

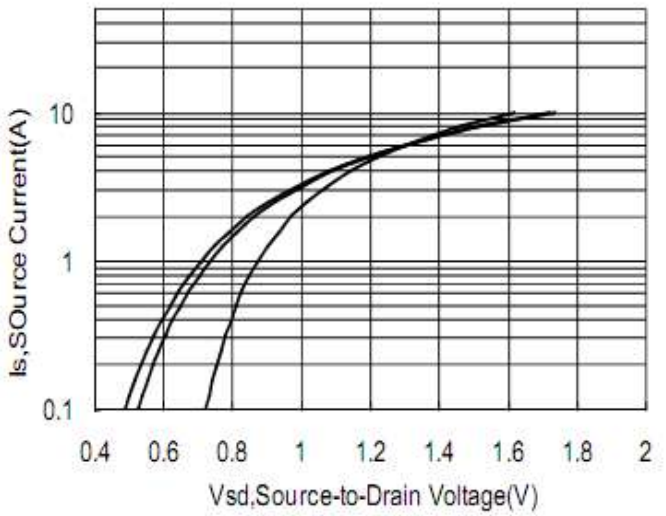


Figure5.Typical Capacitance vs Drain-to-Source Voltage

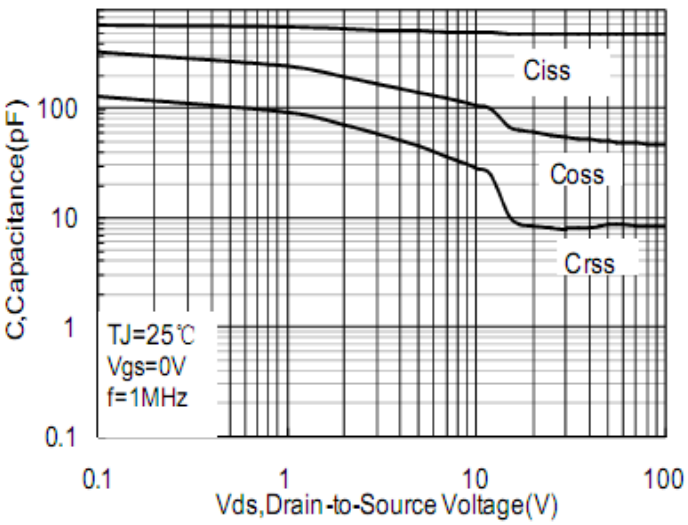


Figure6.Typical Gate Charge vs Gate-to-Source Voltage

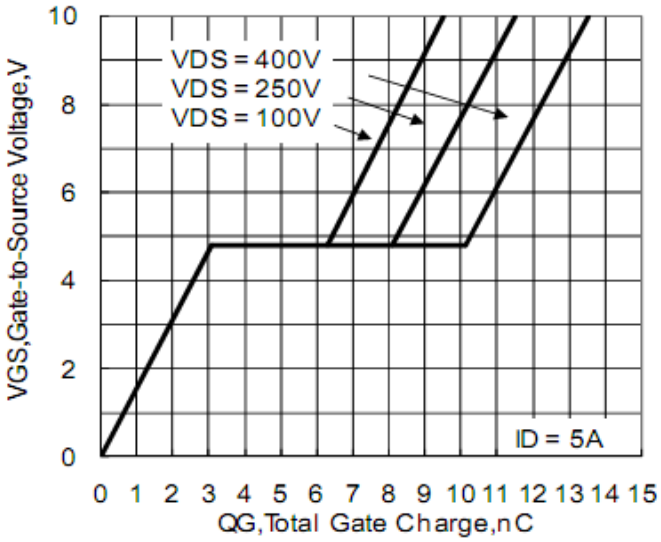


Figure7. Typical Breakdown Voltage vs Junation Temperature

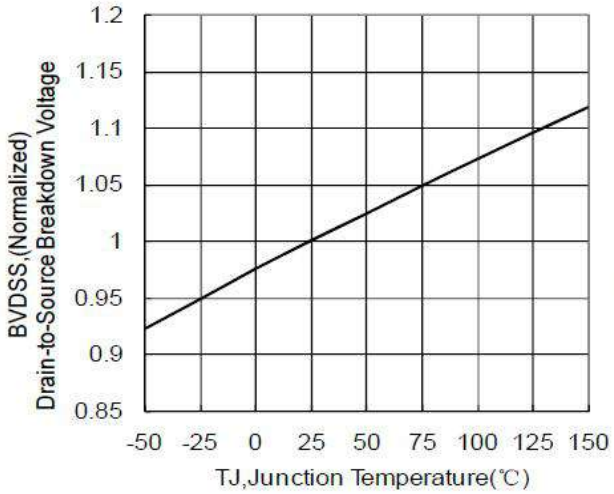


Figure8. Typical Drain-to-Source ON Resistance vs Junction Temperature

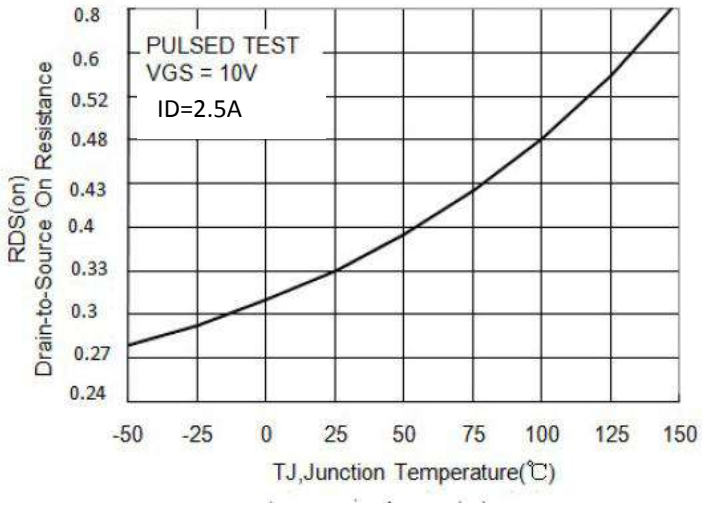


Figure9.Maximum Continuous Drain Current vs Case Temperature

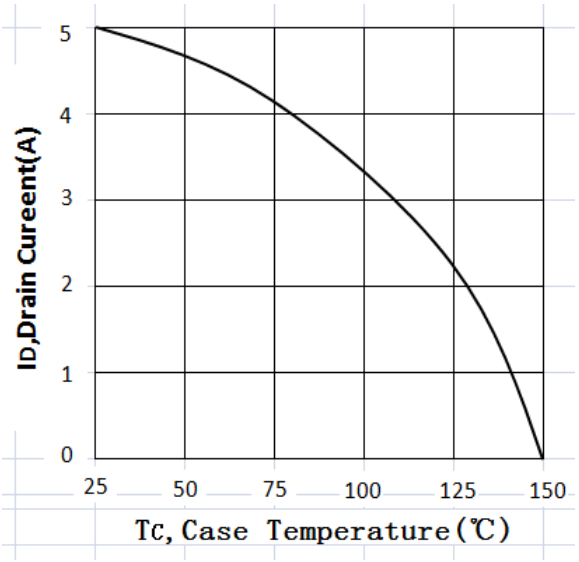
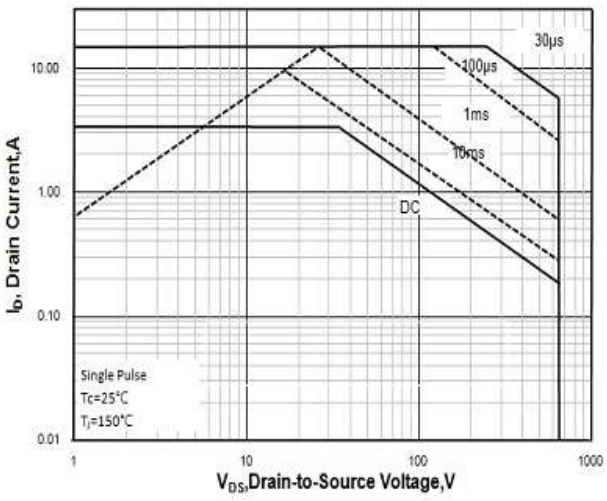


Figure10.Maximum Safe Operating Area



Test Circuits and Waveforms

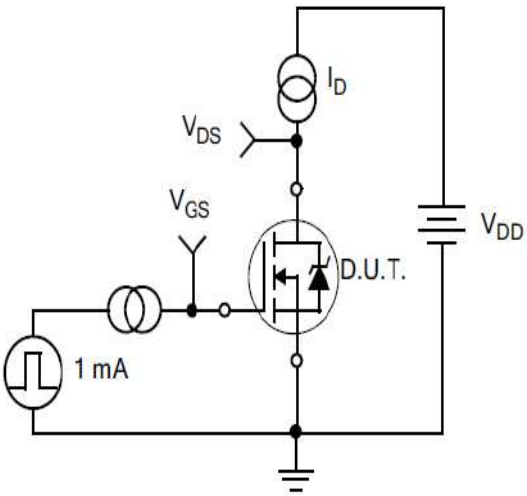


Figure11.
Gate Charge Test Circuit

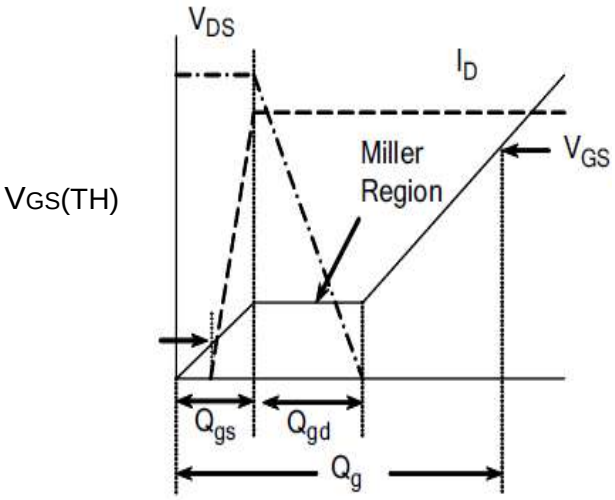


Figure12.
Gate Charge Waveform

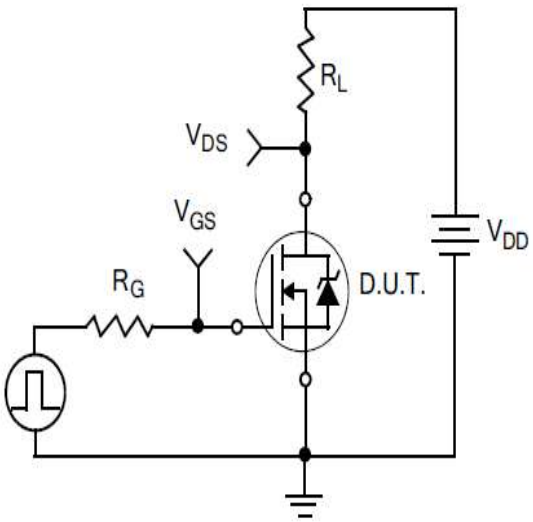


Figure13.
Resistive Switching Test Circuit

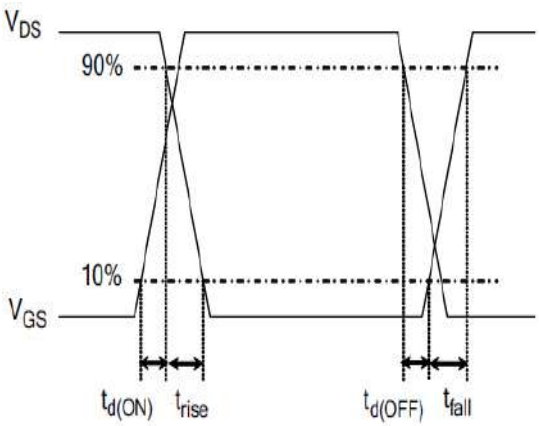


Figure14.
Resistive Switching Waveforms

Test Circuits and Waveforms

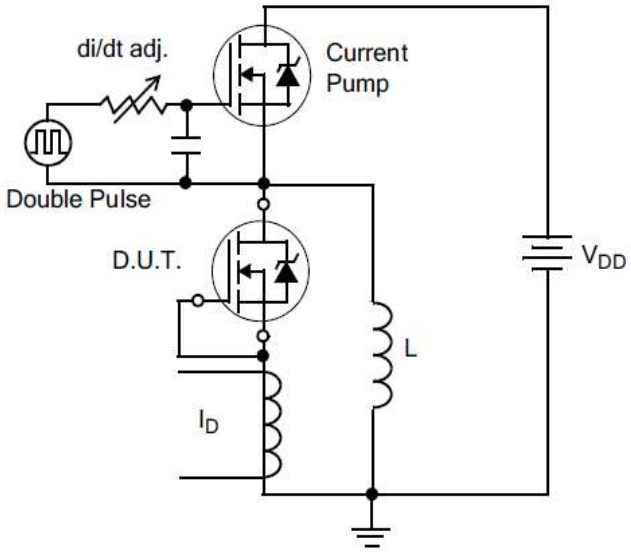


Figure15.Diode Reverse Recovery Test Circuit

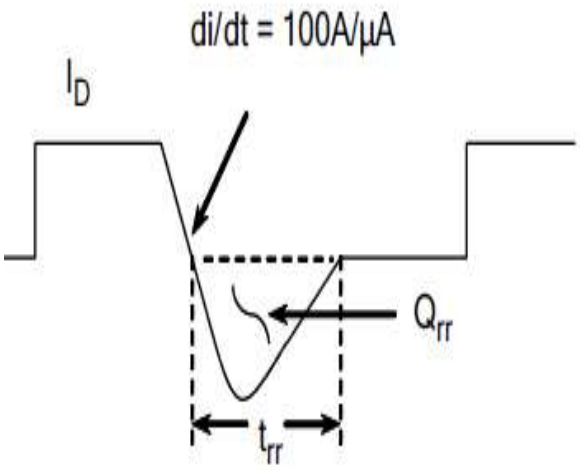


Figure16.Diode Reverse Recovery Waveform

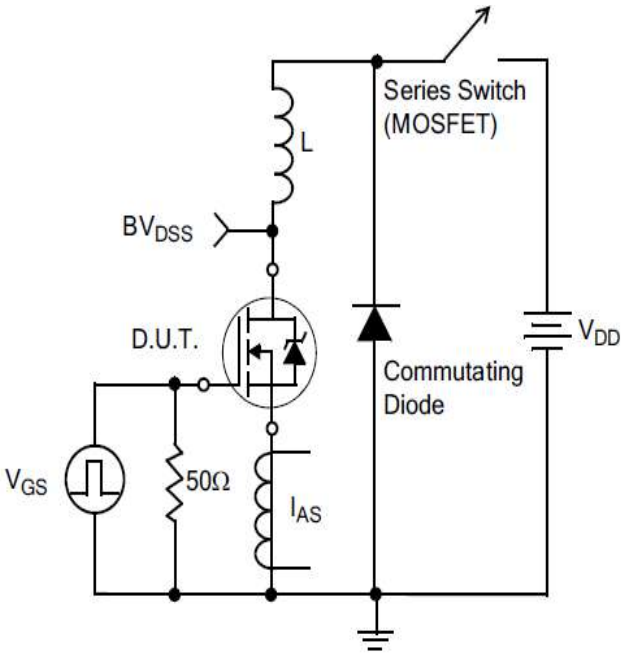
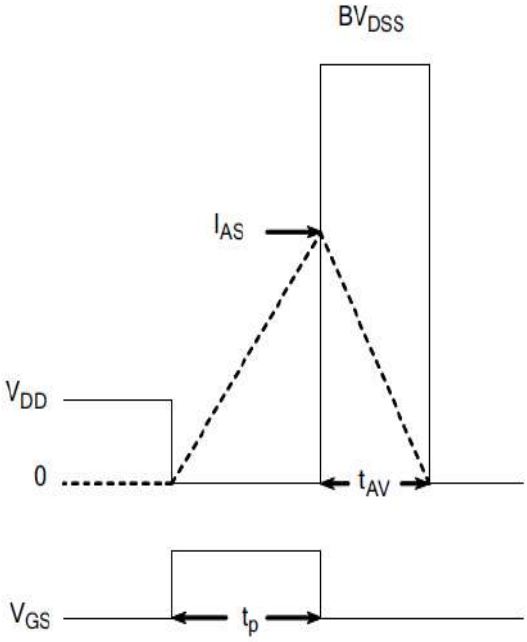


Figure17.Unclamped Inductive Switching Test Circuit



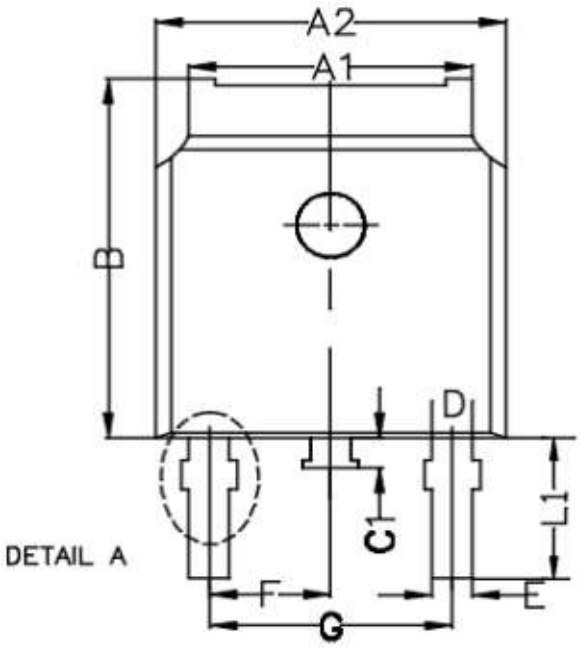
$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

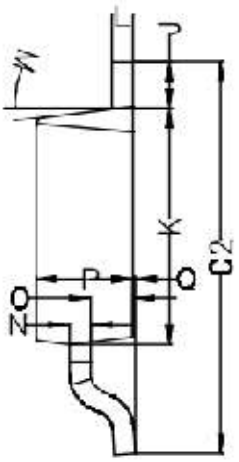
Figure18.Unclamped Inductive Switching Waveforms

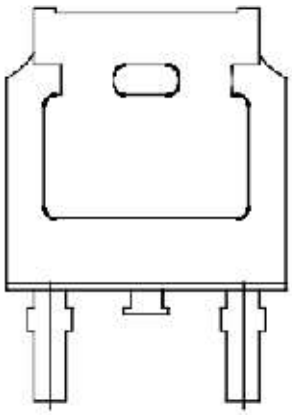
Package outline drawing

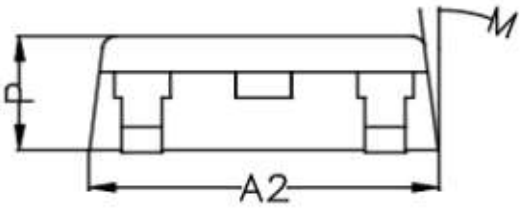
TO-252

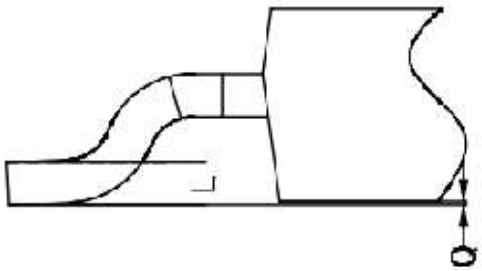
Unit:mm











Symbol	Min	Non	Max
A1	5.22	5.32	5.42
A2	6.55	6.60	6.65
B	7.05	7.10	7.15
C1	0.70	0.80	0.90
C2	9.70	9.90	10.10
D	1.00 REF.		
E	0.76 REF.		
F	2.286 REF.		
G	4.572 REF.		
J	0.95	1.00	1.05
K	6.05	6.10	6.15
L	0.508 REF.		
L1	2.65	2.80	2.95
M	7° REF.		
N	0.508 REF.		
O	0.96	1.01	1.06
P	2.25	2.30	2.35
Q	0.00	0.05	0.10

Disclaimers:

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contr-actual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license eith-er expressed or implied under its patent rights,nor the rights of others.Reproduction of inform-ation in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsi-ble or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all exp-ress or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsi-ble or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as cri-tical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

1.Life support devices or systems are devices or systems which:
- a.are intended for surgical implant into the human body,
- b.support or sustain life,
- c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system,or to affect its safety or effectiveness.