

N Channel MOSFET

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- •PFC stages for server & telecom

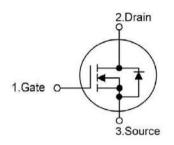
P6

Lead Free Package and Finish

ΙD	Rds(ON)(Typ)	VDSS
4A	1.8Ω	600V



Not to Scale



Features:
•Fast switchi

- Fast switching speed
- •100% avalanche tested
- •Improved dv/dt capability

Ordering Information

Part Number	Package	Marking		
RS4N60F	TO-220F	RS4N60F		

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS4N60F	Units
VDSS	Drain-to-Source Voltage	600	V
ID	Continuous Drain Current (TC = 25°C)	4	
ID	Continuous Drain Current (TC = 100 °C)	1.8	Α
IDM	Pulsed Drain Current (Note*1)	16	1
PD	Power Dissipation(Tc=25°C)	20	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy (Note*2)	88	mJ
IAR	Avalanche Current (Note*1)	4.2	Α
Ear	Repetitive Avalanche Engergy (Note*1)	53	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	${\mathbb C}$
	Operating Junction and Storage		
TJ and TSTG	Temperature Range	-55 to 150	

^{*}Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS4N60F	Units	Test Conditions
RθJC	Junction-to-Case	5	.C\M	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.



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RS4N60F

OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
D) (D 0 0	Drain-to-source Breakdown Voltage	600	-		>	VGS = 0V, ID = 250µA, TJ= 25℃
BVDSS			600		٧	VGS = 0V, ID = 250 μ A, TJ= 150 $^{\circ}$ C
IDSS	Drain-to-Source Leakage Current			1.0	μA	VDS=600V,VGS=0V
IGSS	Gate-to-Source Forward Leakage			100	^	VGS=+30V VDS=0V
	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		1.80	2.20	Ω	VGS=10V,ID=2A
VGS(TH)	Gate Threshold Voltage	3.0		4.0	V	VGS=VDS,ID=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		36			VDS=250V
trise	Rise Time		15		1	ID=4A RG=25Ω
td(OFF)	Turn-OFF Delay Time		90		ns	
tfall	Fall Time		17			VGS=10V

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		537			VGS=0V
Coss	Output Capacitance		55.0		pF	VDS=100V f=1.0MHz
Crss	Reverse Transfer Capacitance		5.0			
Qg	Total Gate Charge		16.0			VDS=480V
Qgs	Gate-to-Source Charge		3.0		nC	ID=4A
Qgd	Gate-to-Drain("Miller") Charge		8.0			VGS=10V

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Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current		-	4	Α	Integral pn-diode
ISM	Maximum Pulsed Current		-	16	Α	in MOSFET
VSD	Diode Forward Voltage		0.9	1.4	V	IS=4A,VGS=0V Tj=25℃
trr	Reverse Recovery Time		320		nS	VGS=0V
Qrr	Reverse Recovery Charge		1.1		μC	IS=4A,di/dt=100A/μs

Notes:

Typical Feature curve $T_J=25^{\circ}C$, unless otherwise noted



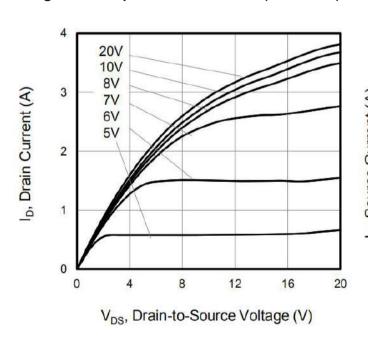
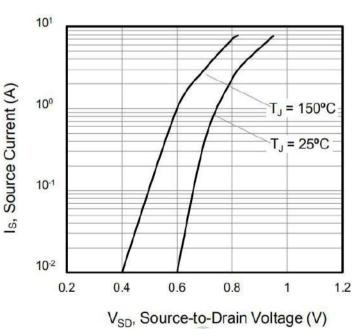


Figure 2. Body Diode Forward Voltage



^{*1.}Repetitive rating; pulse width limited by maximum junction temperature.

^{*2.} IAS = 4A, VDD = 50V, RG = 25Ω , Starting TJ = 25° CPulse width tp limited by Tj,max



Figure 3. Drain Current vs. Temperature

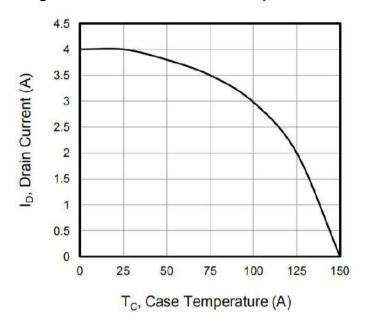


Figure 4. Power Dissipation vs. Temperature

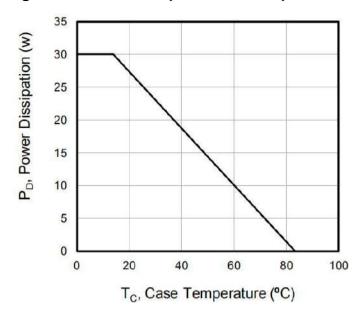


Figure 5. Transfer Characteristics

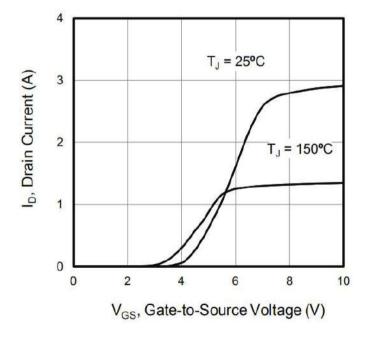
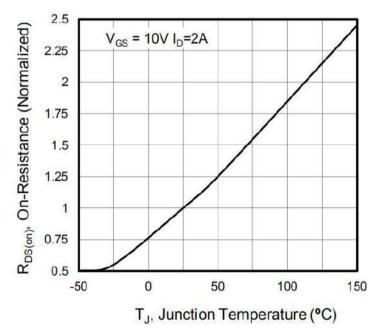
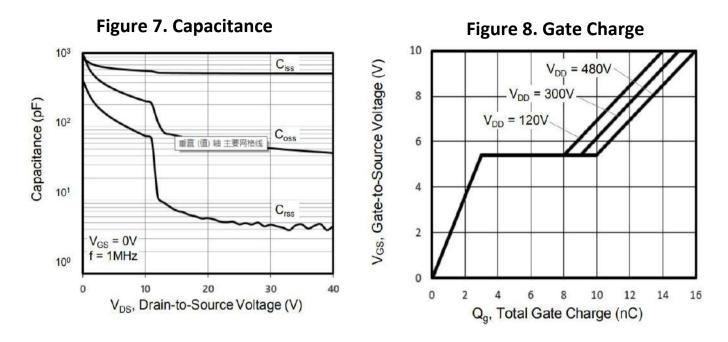


Figure 6. On-Resistance vs. Temperature







TO-220F 10¹ Z_{thJC}, Thermal Impedance (K/W) D = 0.5100 D = 0.2D = 0.1D = 0.05D = 0.02D = 0.0110-1 Single Pulse 10-2 10-6 10-5 10-4 10^{-3} 10-2 10-1 10⁰ T_p, Pulse Width (s)

Figure 9. Transient Thermal Impedance TO-220F



Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

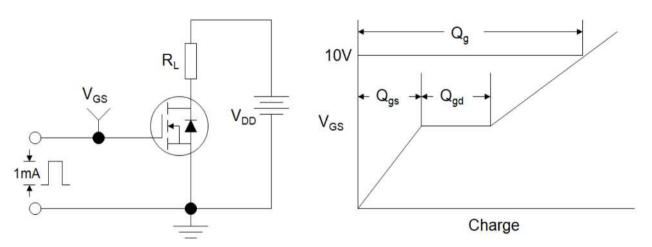


Figure B: Resistive Switching Test Circuit and Waveform

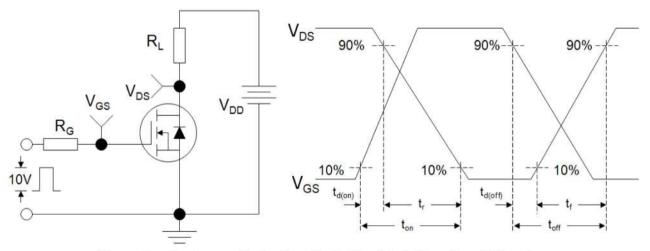
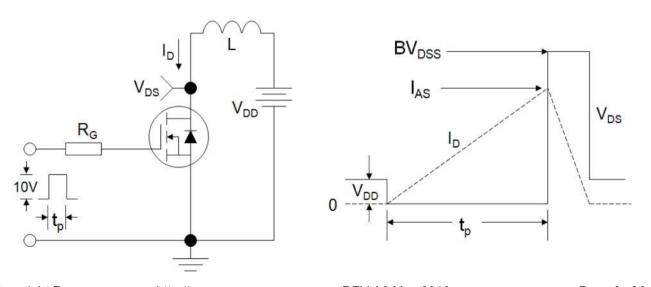


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



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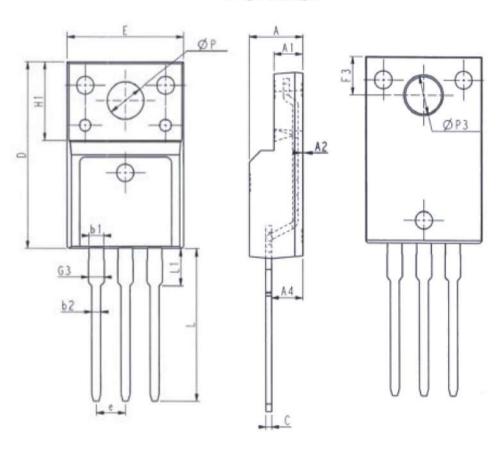
Page 6 of 8



Package outline drawing

Unit:mm

TO-220F



l	Jnit: mn	1	l	Jnit: mm	1		
Symbol	Min.	Max.	Symbol	Symbol Min. Ma			
E	9.96	10.36	L	12. 68	13. 28		
Α	4.50	4. 90	L1	2. 93	3. 13		
A1	2.34	2. 74	Р	3. 03	3. 38		
A2	0.30	0.60	Р3	3. 15	3. 65		
A4	2.56	2.96	F3	3. 15	3. 45		
С	0.40	0.65	G3	1. 25	1. 55		
D	15. 57	16. 17	b1	1.18	1.43		
H1	6. 70	DREF	b2	0.70	0.95		
е	2. 54	4BSC	M.				



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