REASUNOS

RS30N60D

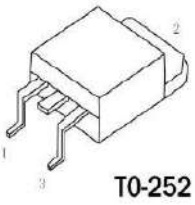
30V N Channel MOSFET

Lead Free Package and Finish

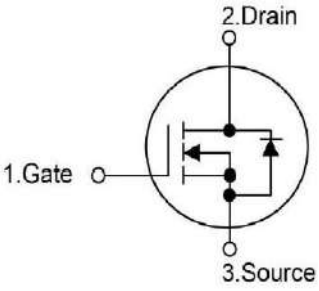
Applications:

- DC-AC inverter Power
- AC-DC Switching Power Supply
- DC-DC Converters

I_D	$R_{DS(ON)}$(Max.)	V_{DSS}
60A	7.5mΩ	30V



Not to Scale



Features:

- $R_{DS(ON)}$=7.5mΩ （Max) @V_{GS}=10V,I_D=25A
- 100% avalanche tested
- High Power and current handing capability
- Simple Drive Requirement

Ordering Information

Part Number	Package	Marking
RS30N60D	TO-252	RS30N60D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS30N60D	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current(Tc=25℃) (Note *1)	60	A
	Continuous Drain Current(Tc=100℃)	35	
IDM	Pulsed Drain Current ((NOTE*2)	140	
PD	Power Dissipation	60	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy ((NOTE*3)	70	mJ
TL	Maximum Temperature for Soldering	300	℃
TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 175	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS30N60D	Units	Test Conditions
RθJC	Junction-to-Case	2.5	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	30	--	--	V	VGS=0V,ID=250μA
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	VDS=30V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+20V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance	--	6.2	7.5	mΩ	VGS=10V,ID=25A
		--	11.5	15	mΩ	VGS=4.5V, ID=20A
VGS(TH)	Gate Threshold Voltage	1.0	1.6	3.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	10	--	nS	VDS=15V RGEN=1.8 Ω ID=20A VGS=10V
trise	Rise Time	--	8	--		
td(OFF)	Turn-OFF Delay Time	--	30	--		
tfall	Fall Time	--	5	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2000	--	pF	VGS=0V VDS=15Vf =1.0MHz
Coss	Output Capacitance	--	280	--		
Crss	Reverse Transfer Capacitance	--	160	--		
Qg	Total Gate Charge	--	23	--	nC	VDS=10V ID=25A VGS=10V
Qgs	Gate-to-Source Charge	--	7	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	4.5	--		

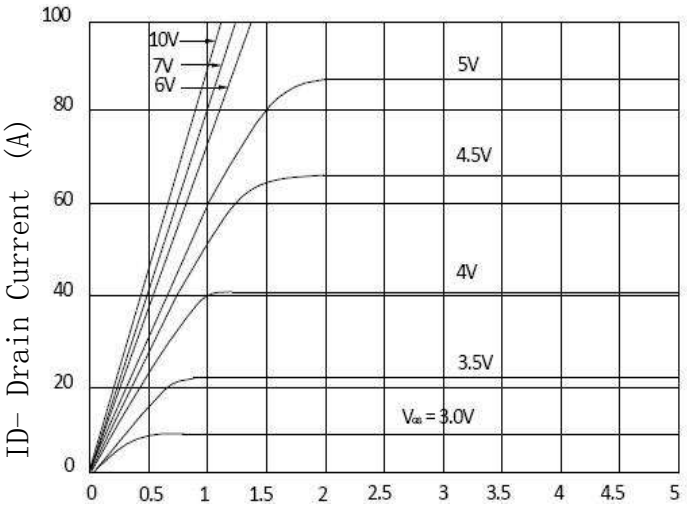
Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current (NOTE*4)	--	--	60	A	Integral pn-diode in MOSFET
ISM	Maximum Pulsed Current	--	--	250	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=8A,VGS=0V
trr	Reverse Recovery Time	--	22	--	ns	VGS=0V IF=16A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	12	--	μC	

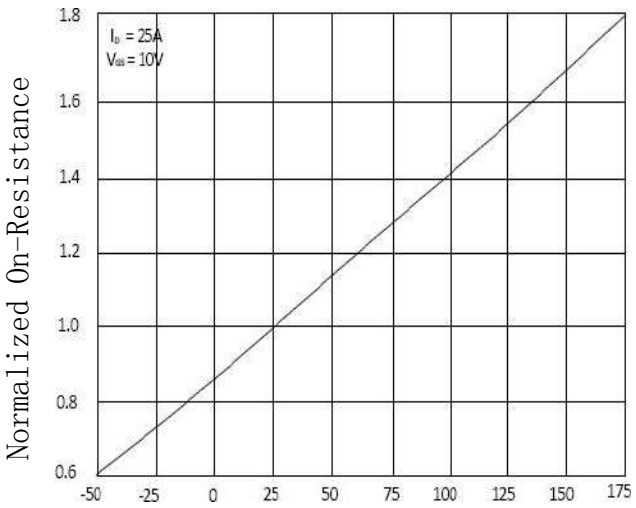
Notes:

*1.The maximum current rating is package limited.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.EAS condition: TJ=25℃,VDD=15V,VG=10V, RG=25Ω，L=1mH.

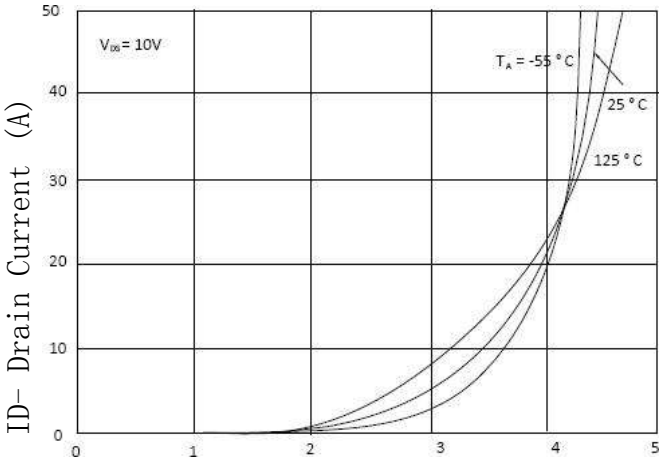
Typical Electrical And Thermal Characteristics (Curves)



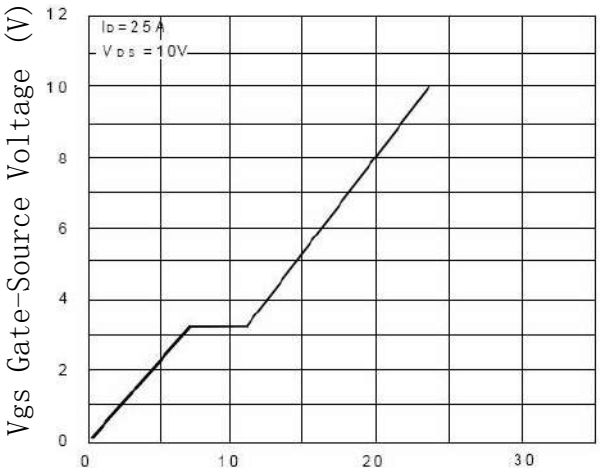
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



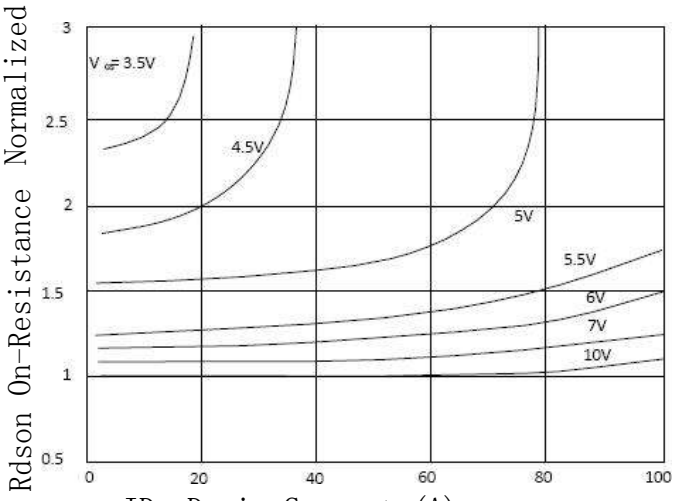
TJ-Junction Temperature(℃)
Figure 4 Rdson-JunctionTemperature



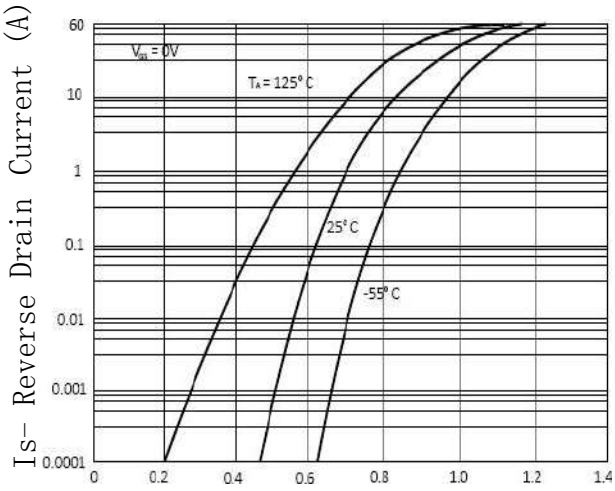
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



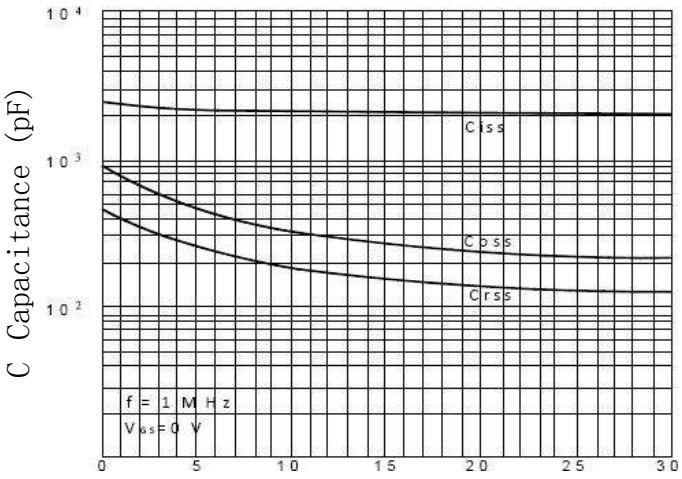
Qg Gate Charge (nC)
Figure 5 Gate Charge



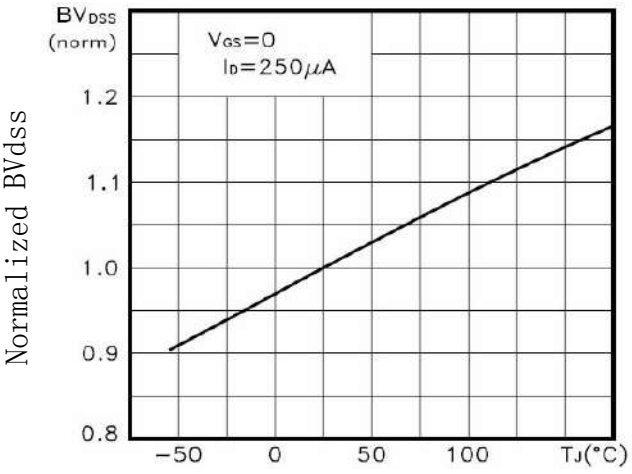
ID- Drain Current (A)
Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



TJ-Junction Temperature(℃)
Figure 9 BVDSS vs Junction Temperature

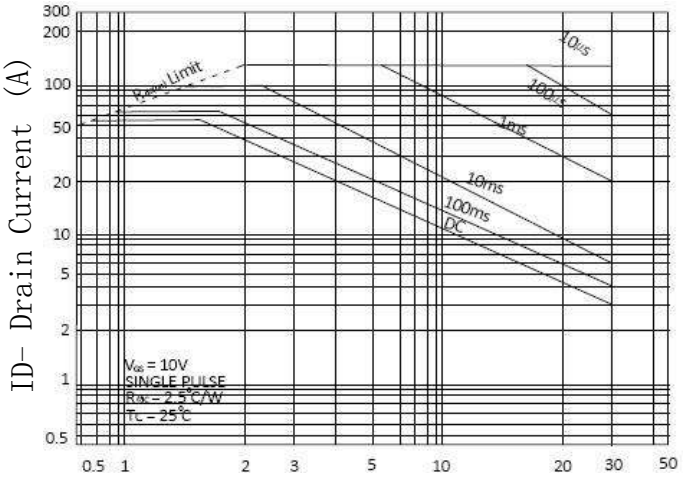
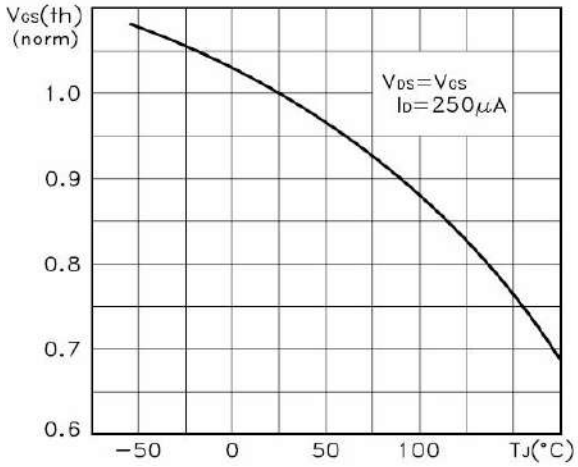
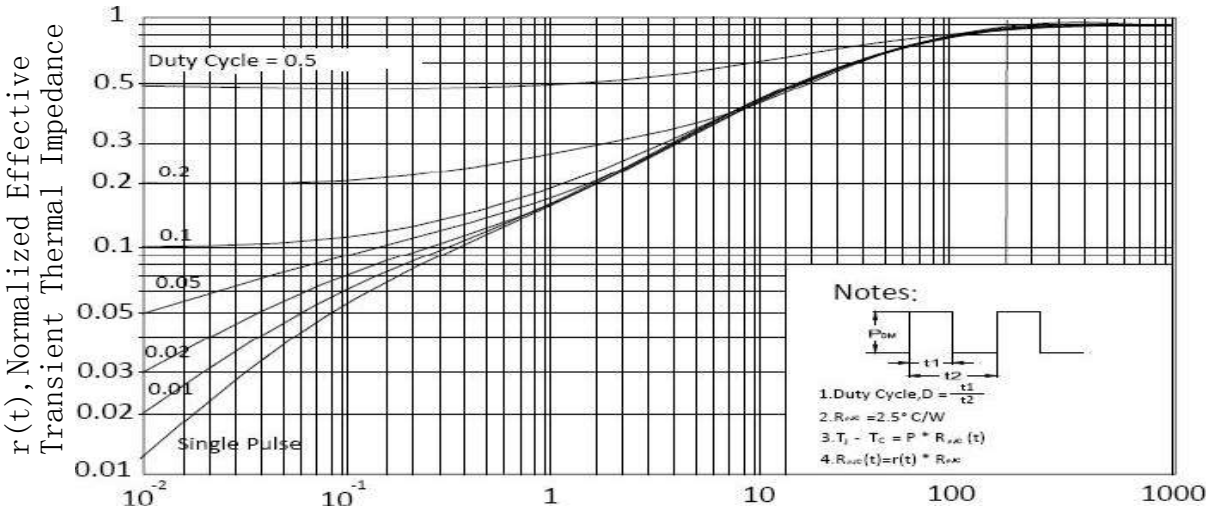


Figure 8 Safe Operation Area



TJ-Junction Temperature(℃)

Figure 10 VGS(th) vs Junction Temperature

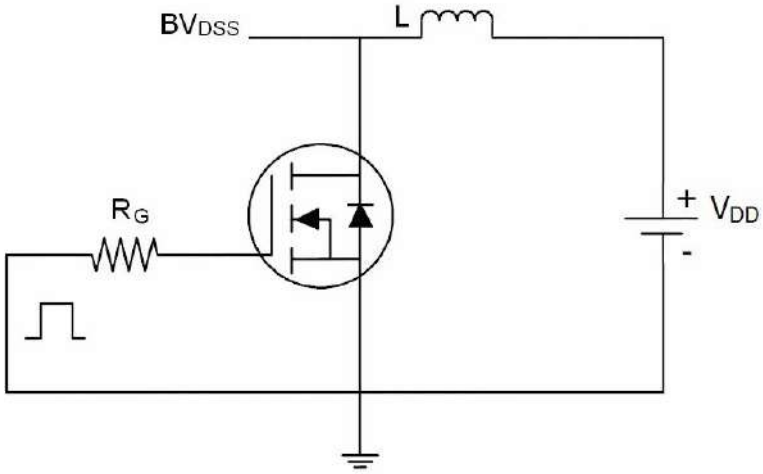


Square Wave Pluse Duration(sec)

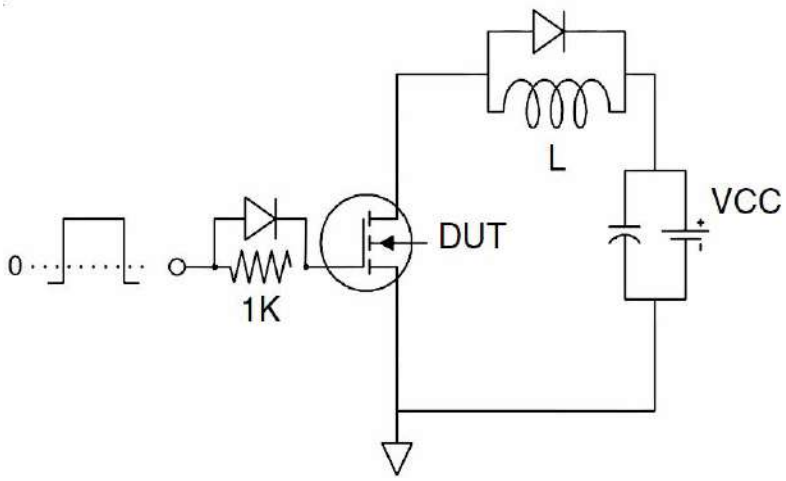
Figure 11 Normalized Maximum Transient Thermal Impedance

Test circuit

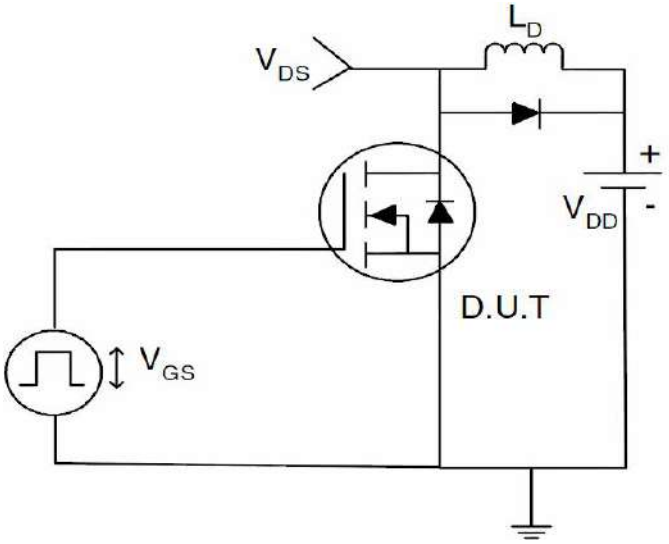
1) EAS test Circuits



2) Gate charge test Circuit:

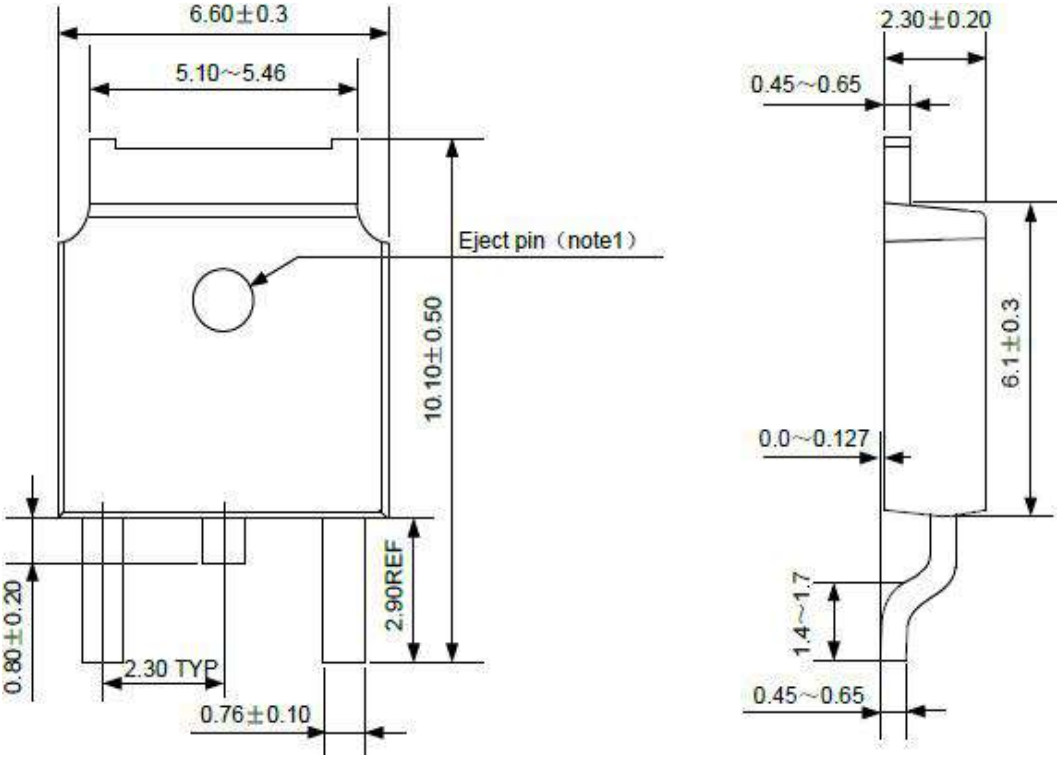


3) Switch Time Test Circuit:



Package outline drawing

Unit:mm



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