N Channel MOSFET

Lead Free Package and Finish

Applications:

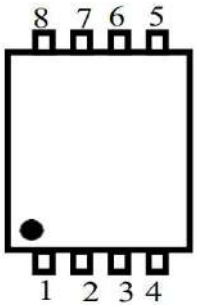
- PWM applications
- Load switch
- Power management

I_D	$R_{DS(ON)}$(Max.)	V_{DSS}
50A	5.5mΩ	30V

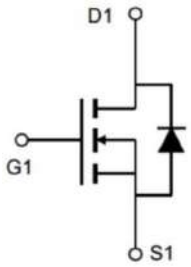
Features:

- V_{DS}=30V; I_D=50A
  $R_{DS(ON)}$ < 5.5mΩ @ V_{GS} =10V
  Rds(on) < 7.5mΩ @ VGS =4.5V
- Ultra Low On-Resistance
- High UIS and UIS 100% Test
- RoHS Compliant

PDFN3X3



Marking and pin Assignment



Schematic Diagram

Ordering Informat ion

Part Number	Package	Marking
RS30N50K	PDFN3×3	RS30N50K

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS30N50K	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current（Tc=25℃）	50	A
	Continuous Drain Current Tc=100℃	30	
IDM	Pulsed Drain Current (Note*1)	90	
PD	Power Dissipation（Tc=25℃）	35	W
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy (Note*2)	55	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS30N50K	Units	Test Conditions
RθJA	Thermal Resistance- Junction to Ambient	62.5	℃/W	Surface Mounted on 1 in2 pad area, t ≤ 10 sec
RθJC	Thermal Resistance- Junction to Case	3.57		

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	30	--	--	V	VGS=0V,ID=250μA
IDSS	Drain-to-Source Leakage Current	--	--	1	μA	VDS=30V,VGS=0V
IGSS	Gate-to-Source Forward Leakage	--	--	100	nA	VGS=+20V VDS=0V
	Gate-to-Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (Note*3)	--	3.8	5.5	mΩ	VGS=10V,ID=10A
		--	5.5	7.5	mΩ	VGS=4.5V,ID=5A
VGS(TH)	Gate Threshold Voltage	1.0	1.5	2.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	--	7	--	nS	VDS=15V VGS=10V ID=10A RG=4.5Ω RL = 1.5 Ω
trise	Rise Time	--	30	--		
td(OFF)	Turn-OFF Delay Time	--	19	--		
tfall	Fall Time	--	19	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1148	--	pF	VGS=0V VDS=10V f=1.0MHz
Coss	Output Capacitance	--	109	--		
Crss	Reverse Transfer Capacitance	--	89	--		
Qg	Total Gate Charge	--	23	--	nC	VDS=15V ID=10A VGS=10V
Qgs	Gate-to-Source Charge	--	5.6	--		
Qgd	Gate-to-Drain("Miller"）Charge	--	3.3	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{SD}	Source-Drain Current(Body Diode)	--	--	50	A	
I_{SDM}	Pulsed Source-Drain Current(Body Diode)	--	--	90	A	Maximum Pulsed Drain to Source Diode Forward Current
V_{SD}	Diode Forward Voltage	--	--	1.3	V	IS=34A,VGS=0V
trr	Reverse Recovery Time	--	34	--	nS	VGS=0V I_F=10A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	7.2	--	μC	

Notes:

*1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
*2. EAS condition: TJ=25℃, VGS=10V, RG=25Ω，L=0.5mH
*3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Feature curve

Figure 1. Output Characteristics (TJ = 25ºC)

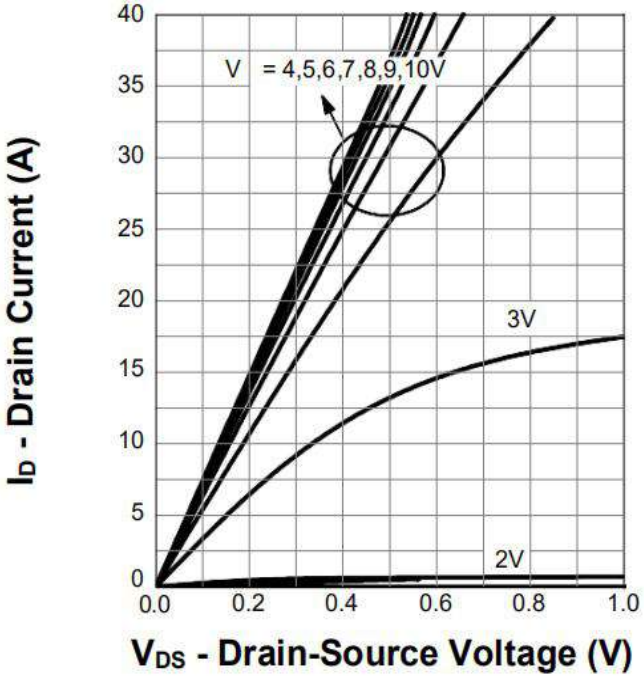


Figure 2. Transfer Characteristics

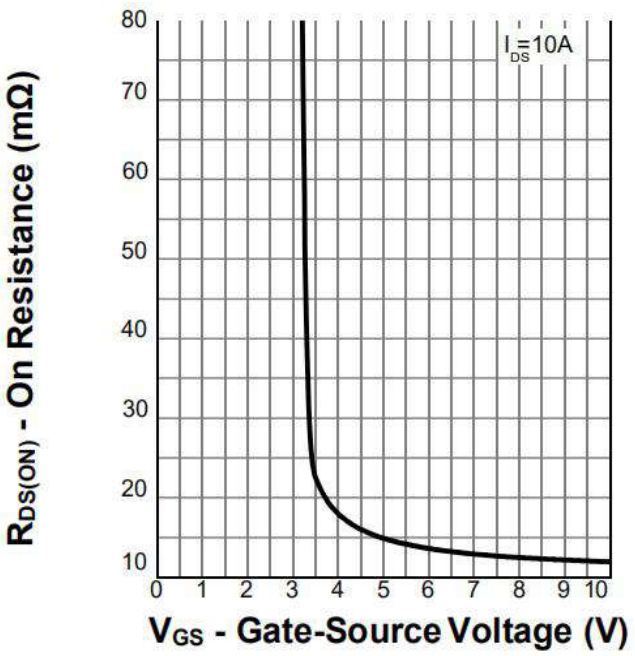


Figure 3. On-Resistance vs. Drain Current

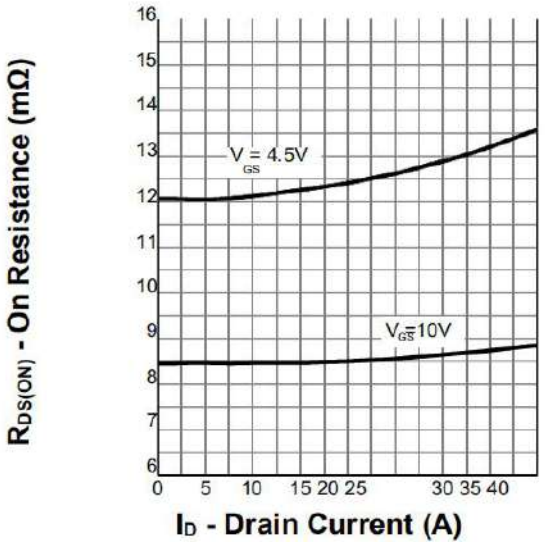


Figure 4: Body Diode Characteristics

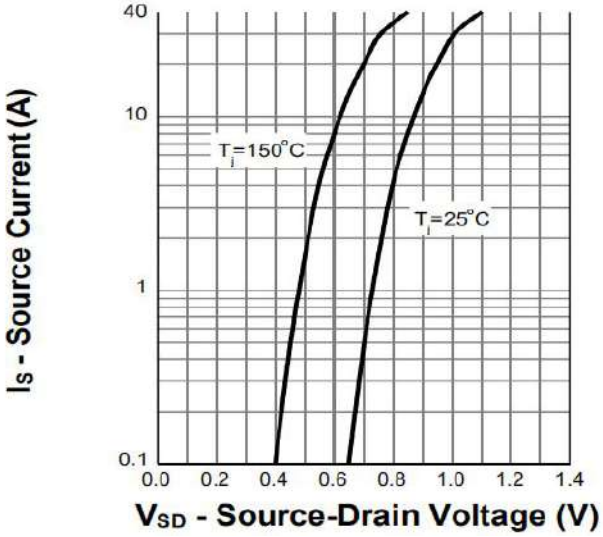


Figure 5. Gate Charge Characteristics

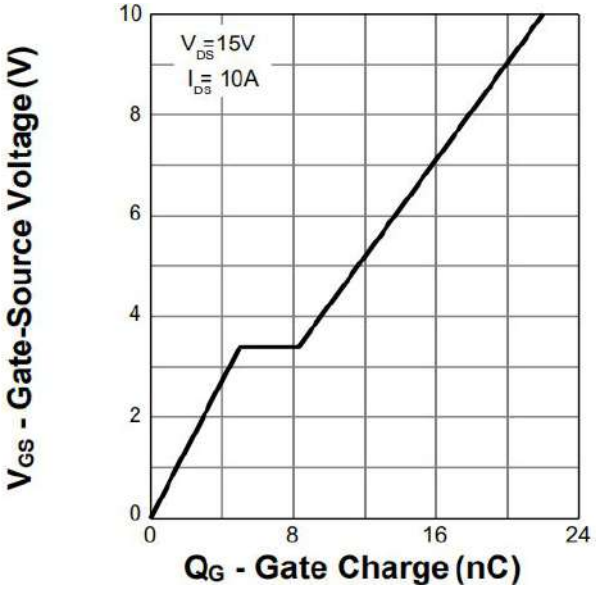


Figure 6. Capacitance Characteristics

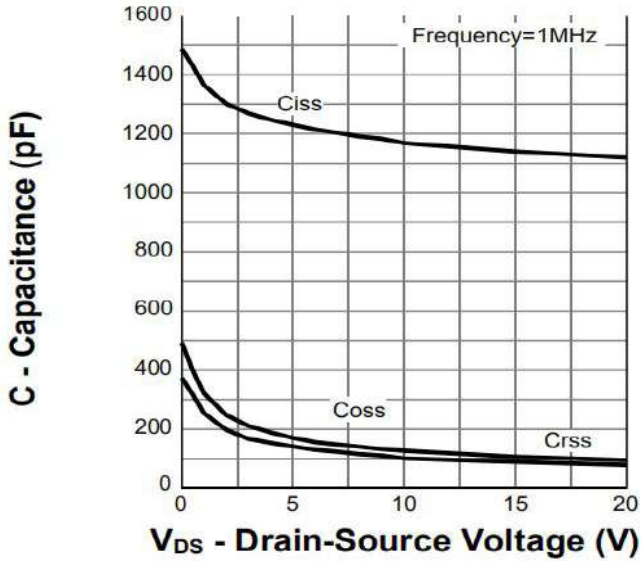


Figure 7:Normalized Threshold Voltage vs. Junction Temperature

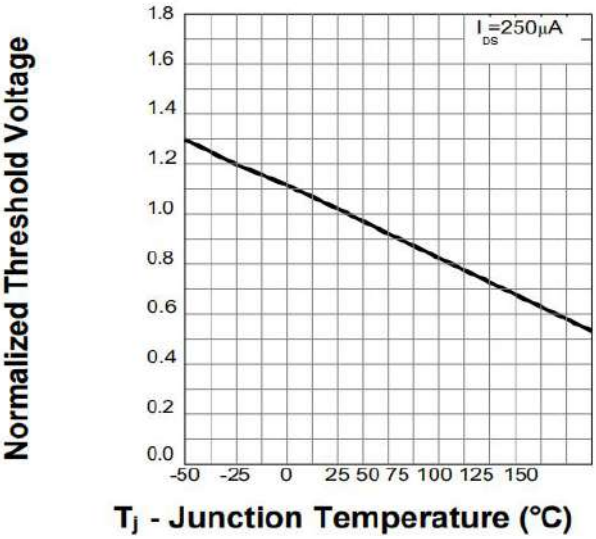


Figure 8: Normalized on Resistance vs. Junction Temperature

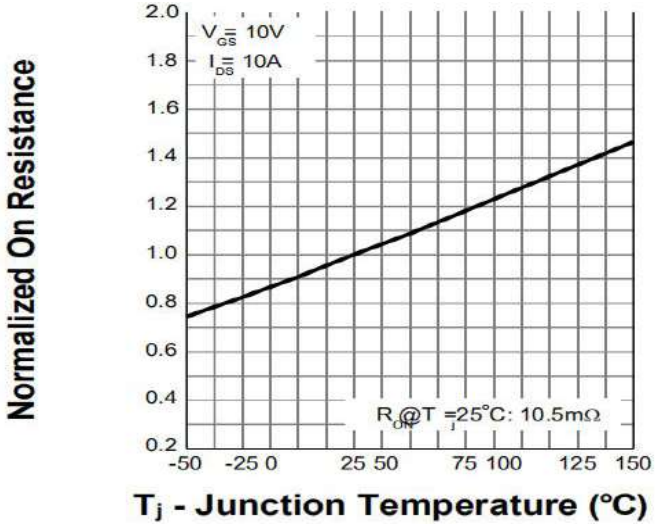


Figure 9: Maximum Safe Operating Area

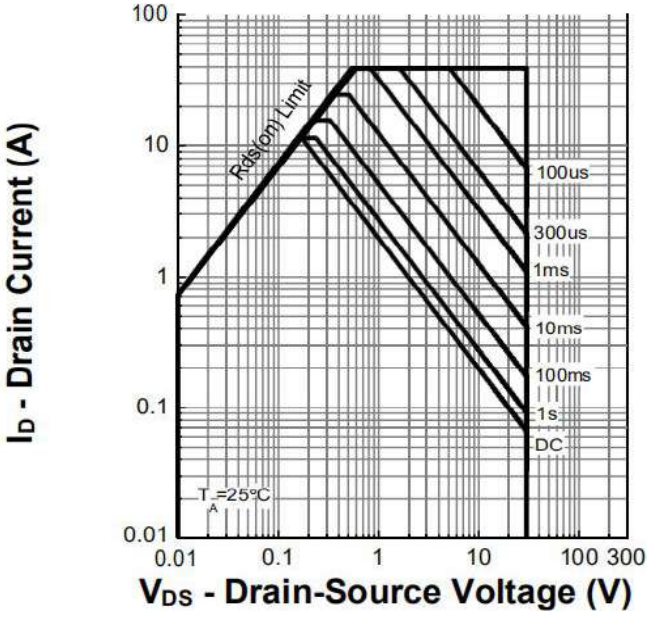


Figure 9: Maximum Safe Operating Area

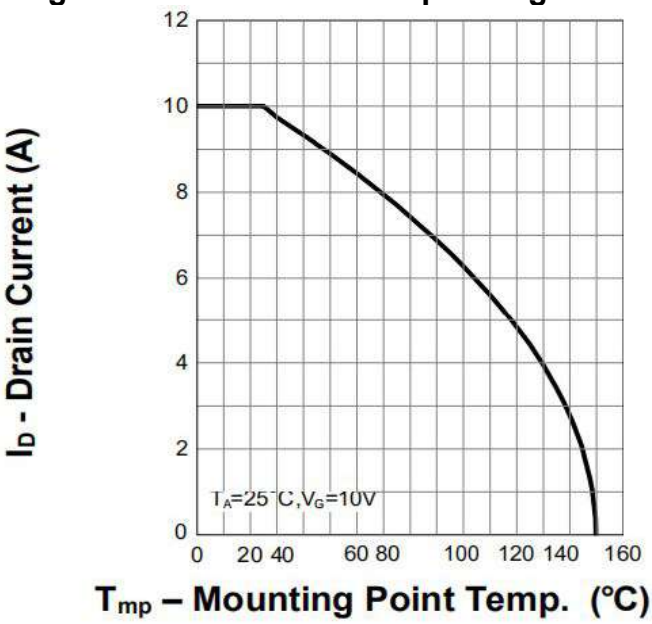
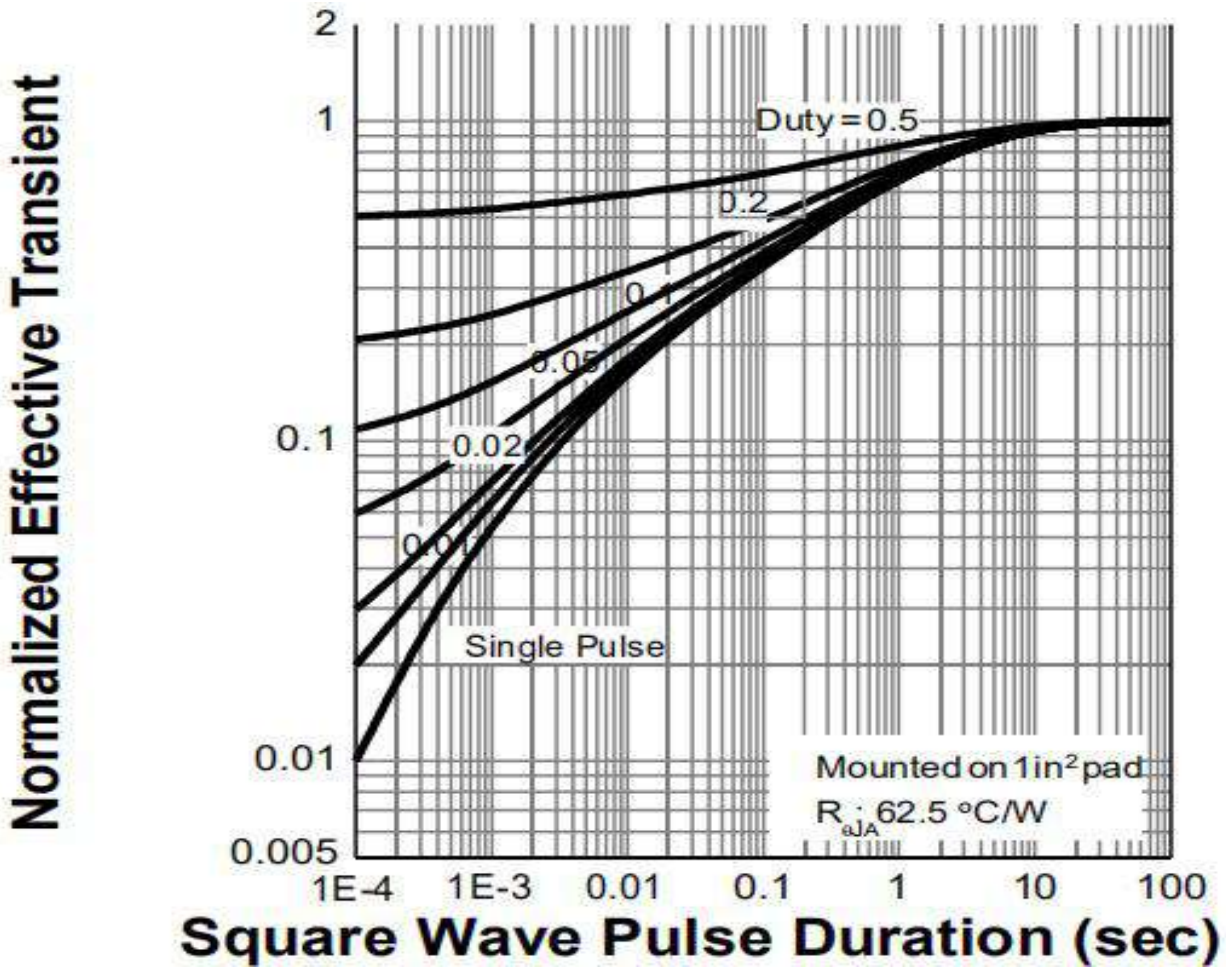


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuits and Waveforms

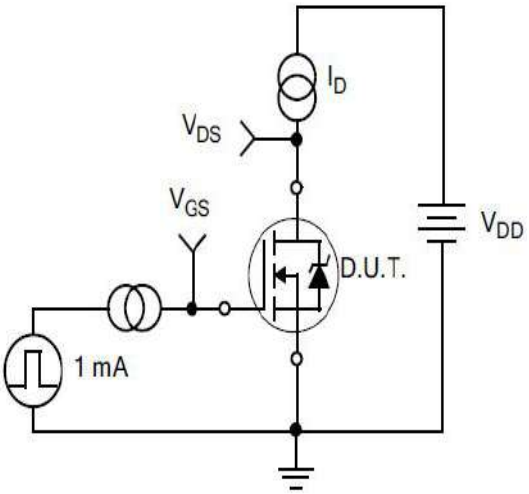


Figure A.
Gate Charge Test Circuit

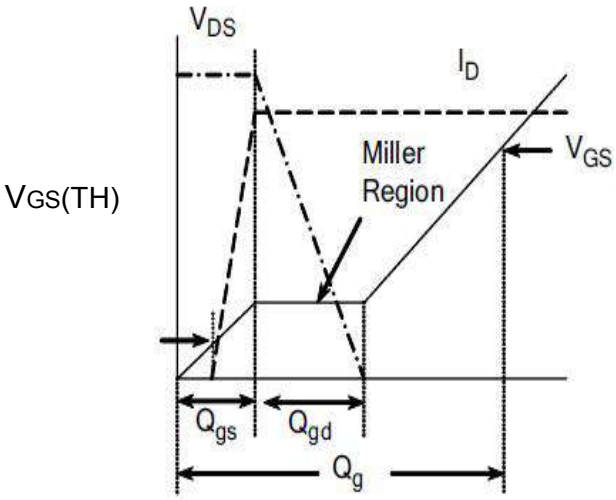


Figure B.
Gate Charge Waveform

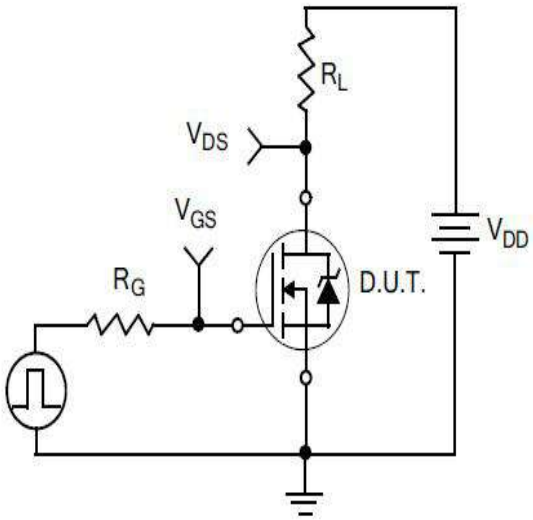


Figure C.
Resistive Switching Test Circuit

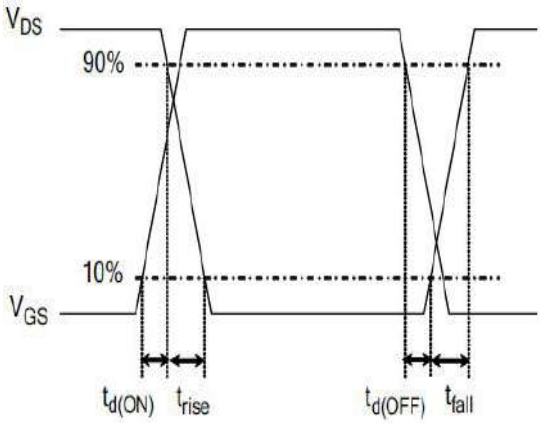


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

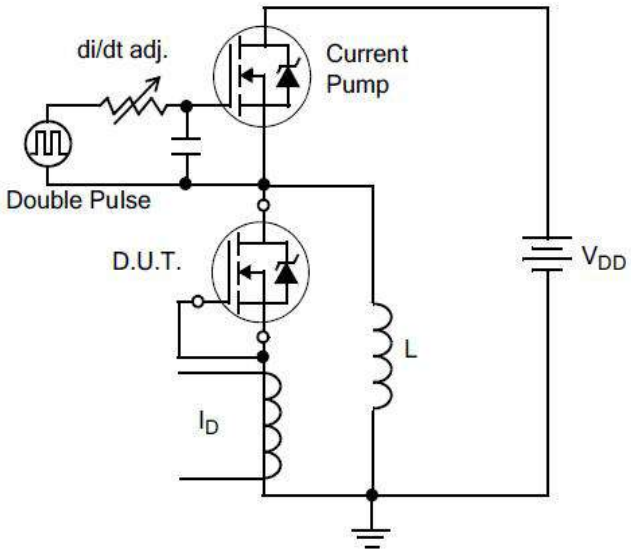


Figure E.Diode Reverse Recovery Test Circuit

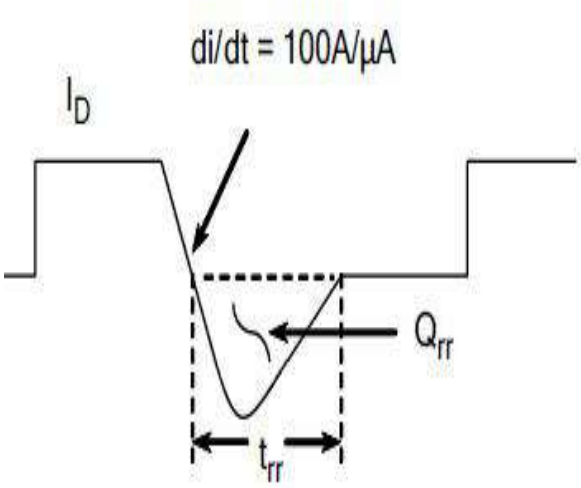


Figure F.Diode Reverse Recovery Waveform

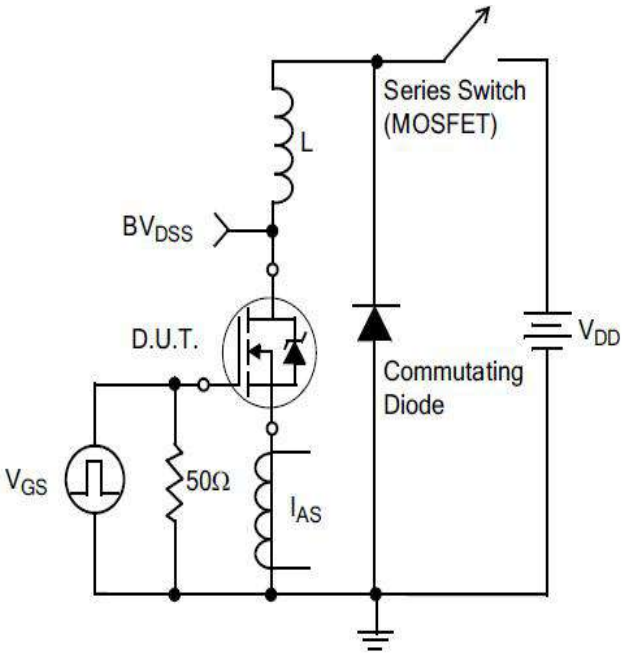
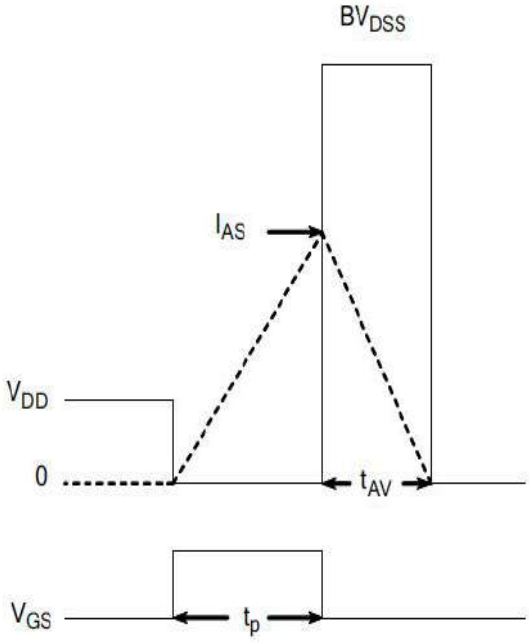


Figure G.Unclamped Inductive Switching Test Circuit

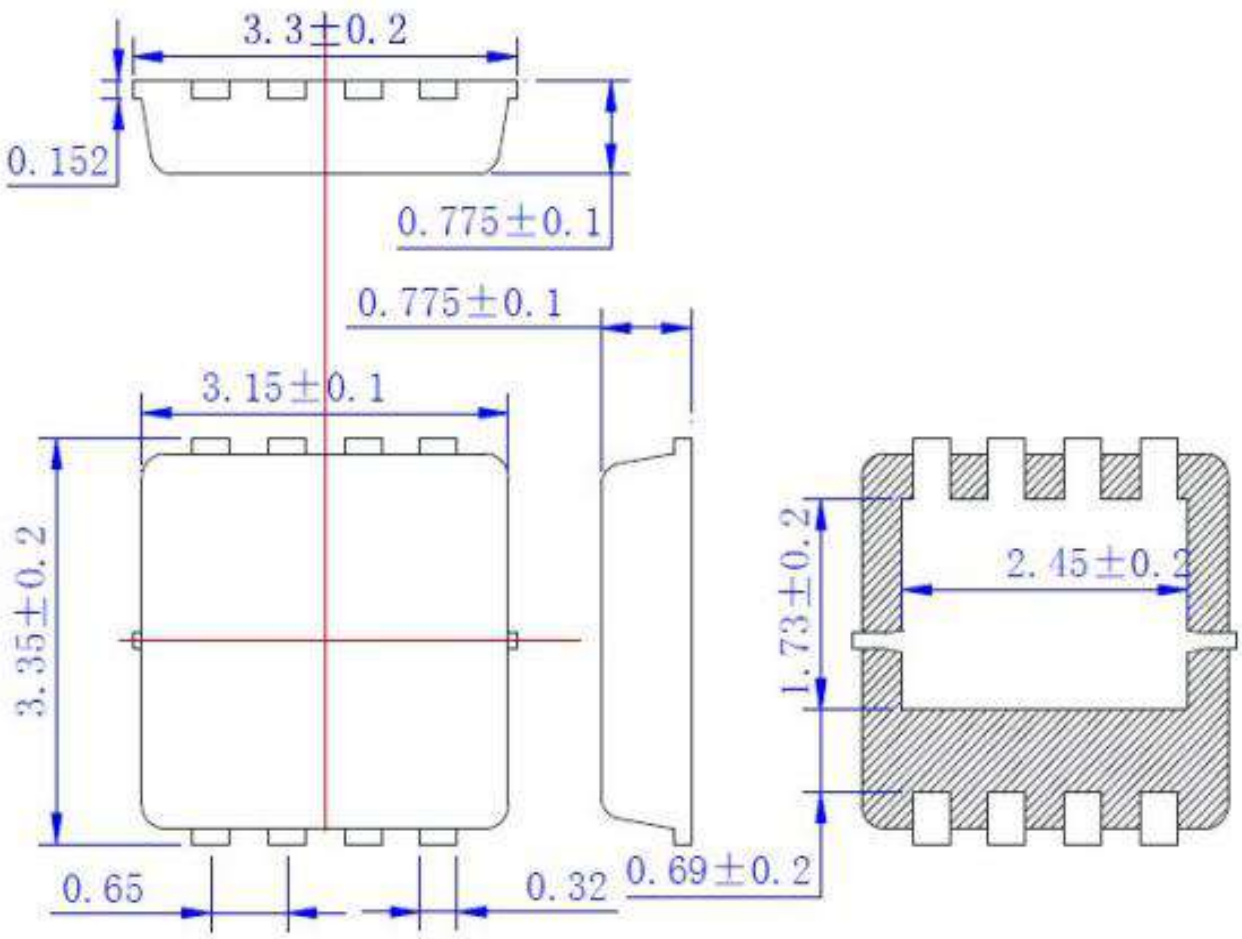


$$E_{AS}= \frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing

Package Mechanical Data- PDFN3.3X3.3-8L



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