

#### **N Channel MOSFET**

## **Applications:**

- Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

#### Features:

- •Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

## Ordering Information

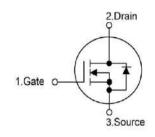
Part Number	Package	Marking
RS2N65F	TO-220F	RS2N65F



Lead Free Package and Finish

ΙD	Rds(ON)(Typ.)	VDSS
2.0A	4.1Ω	650V





Not to Scale

## Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS2N65F	Units	
VDSS	Drain-to-Source Voltage (Note*1)	650	V	
ID	Continuous Drain Current	2.0		
ID@ 100 ℃	Continuous Drain Current	1.3	А	
lом	Pulsed Drain Current (Note*2)	6.0		
DD	Power Dissipation	25	W	
PD	Derating Factor above 25℃	0.28	W/°C	
VGS	Gate-to-Source Voltage	±30	V	
EAS	Single Pulse Avalanche Engergy L=30mH IAS=2.52A VDD=145V RG=25Ω TJ=25℃	28.8	mJ	
	Maximum Temperature for Soldering			
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	°C	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150		

<sup>\*</sup>Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

## **Thermal Resistance**

Symbol	Parameter	RS2N65F	Units	Test Conditions
Rejc	Junction-to-Case	1.92	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
Reja	Junction-to-Ambient	62.5	]	1 cubic foot chamber,free air.

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## **OFF Characteristics** TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650			٧	Vgs=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1.0	μΑ	V <sub>DS</sub> =650V,V <sub>GS</sub> =0V
Igss	Gate-to-Source Forward Leakage			100	nΛ	Vgs=+30V Vds=0V
1633	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

# ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		4.1	4.8	Ω	Vgs=10V,lb=1A
$V_{GS(TH)}$	Gate Threshold Voltage	3.0		4.0	V	Vgs=Vds,Id=250µA

# Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		7.8			VDS=300V
trise	Rise Time		33		nS	ID=2.0A
td(OFF)	Turn-OFF Delay Time		23		113	RG=25Ω
tfall	Fall Time		59			(Note:3,4)

## **Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		310			Vgs=0V
Coss	Output Capacitance		39		pF	Vps=25V
Crss	Reverse Transfer Capacitance		6			f=1.0MHz
Qg	Total Gate Charge		8			Vps=520V
Qgs	Gate-to-Source Charge		1.2		nC	ID=2.0A VGS=10V
Qgd	Gate-to-Drain("Miller") Charge		5			(Note:3,4)

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### **Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current			2	Α	Integral pn-diode
Ism	Maximum Pulsed Current			8	Α	in MOSFET
Vsd	Diode Forward Voltage			1.4	V	Is=2.0A,Vgs=0V
trr	Reverse Recovery Time		80		nS	Vgs=0V
Qrr	Reverse Recovery Charge		1.8		μC	Is=2.0A,di/dt=100A/µs

#### Notes:

# **Typical Feature curve** (TJ = 25°C, unless otherwise noted)

Figure 1. Output Characteristics

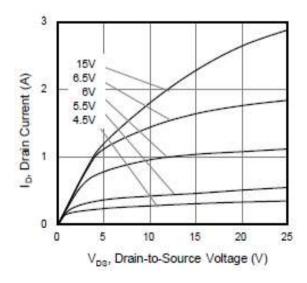
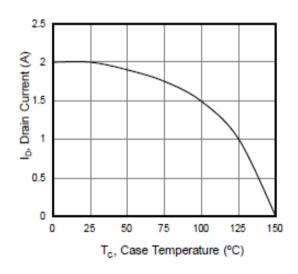


Figure 2. Drain Current vs. Temperature



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<sup>\*1.</sup>TJ=±25°C to +150°C.

<sup>\*2.</sup>Repetitive rating; pulse width limited by maximum junction temperature.

<sup>\*3.</sup>Pulse width≤300µs;duty cycle ≤1%.

<sup>\*4.</sup>Basically not affected by temperature.



Figure 3. Body Diode Forward Voltage

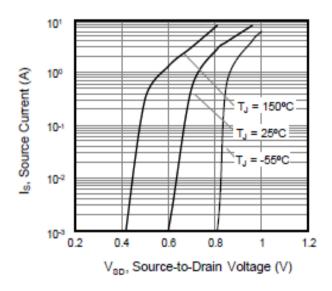


Figure 4. Power Dissipation vs. Temperature

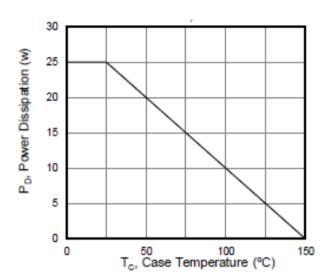


Figure 5. On-Resistance vs. Temperature

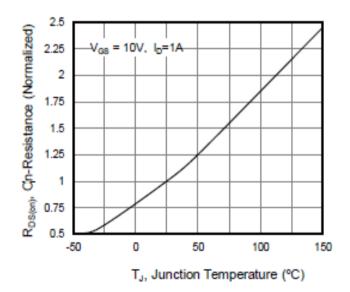
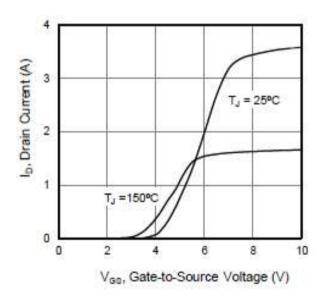


Figure 6. Transfer Characteristics



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Figure7. Capacitance

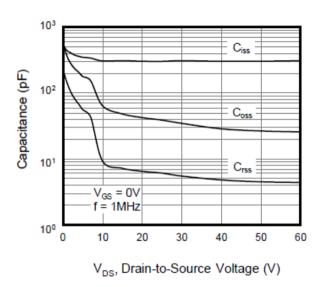
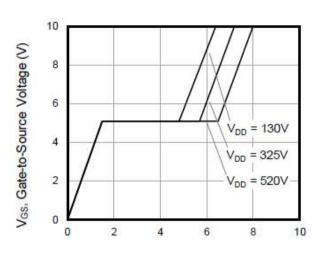
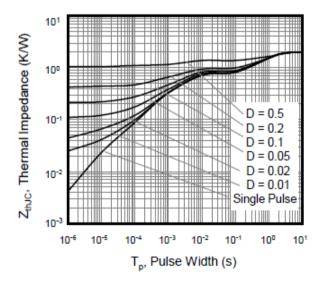


Figure8. Gate Charge



Q<sub>o</sub>, Total Gate Charge (nC)

Figure 9. Transient Thermal Impedance TO-220F





## **Test Circuits and Waveforms**

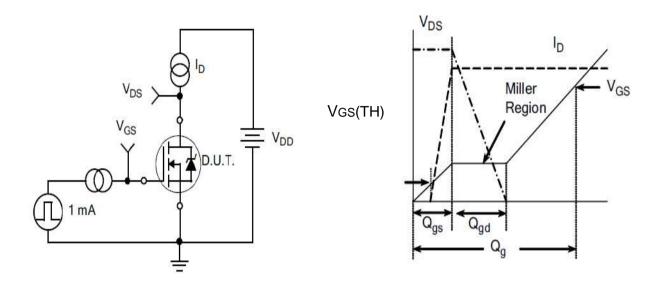


Figure 10.
Gate Charge Test Circuit

Figure 11.
Gate Charge Waveform

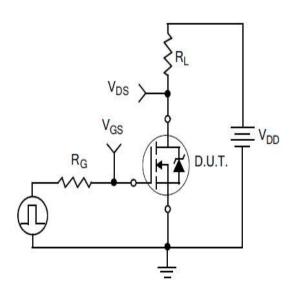


Figure 12.
Resistive Switching Test Circuit

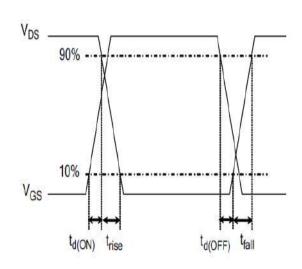


Figure 13.
Resistive Switching Waveforms



## **Test Circuits and Waveforms**

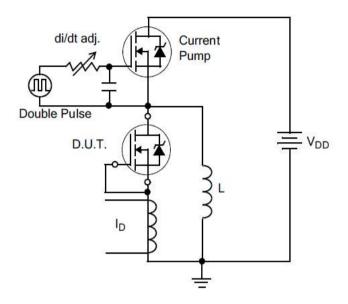


Figure 14. Diode Reverse Recovery
Test Circuit

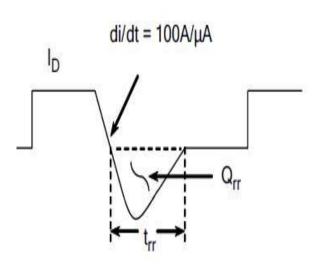


Figure 15. Diode Reverse Recovery Waveform

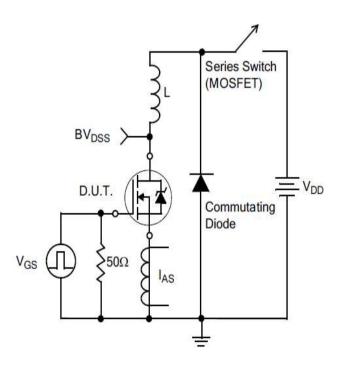
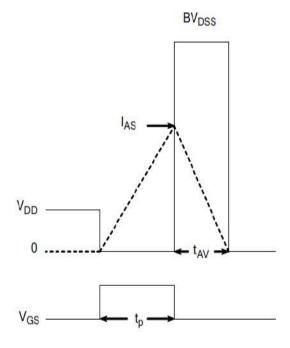


Figure 16. Unclamped Inductive Switching Test Circuit

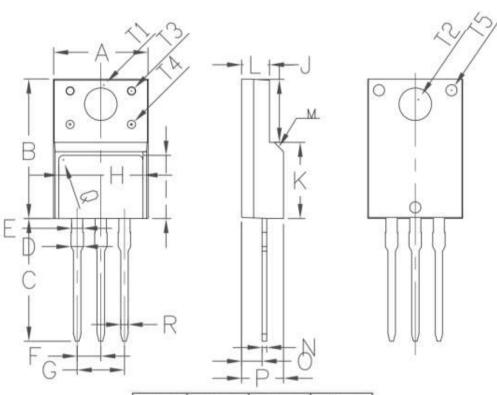


$$EAS = \frac{IAS^2L}{2}$$

Figure 17. Unclamped Inductive Switching Waveforms

# Package outline drawing





Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
C	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
H	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K		9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
0	2.15	2, 35	2.55
P	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3. 45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83



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  - b.support or sustain life,
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