RS2N60F

N Channel MOSFET

Applications:

- •Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

Features:

- •Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

Ordering Information

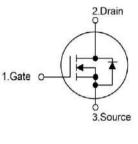
Part Number	Package	Marking
RS2N60F	TO-220F	RS2N60F



Lead Free Package and Finish

lo	RDS(ON)(Typ.)	Vdss
2.0A	3.7Ω	600V





Not to Scale

Absolute Maximun Ratings Tc=25°C unless otherwise specified

Symbol	Parameter	RS2N60F	Units	
VDSS	Drain-to-Source Voltage (Note*1)	600	V	
ID	Continuous Drain Current	2.0		
ID@ 100 ℃	Continuous Drain Current	1.3	А	
IDM	Pulsed Drain Current (Note*2)	8.0		
DD	Power Dissipation	25	W	
PD	Derating Factor above 25℃	0.28	W/℃	
VGS	Gate-to-Source Voltage	±20	V	
EAS	Single Pulse Avalanche Engergy L=30mH IAS=2.52A VDD=145V RG=25Ω TJ=25℃	57	mJ	
	Maximum Temperature for Soldering			
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	°C	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150		

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS2N60F	Units	Test Conditions
Rejc	Junction-to-Case	1.98	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.



OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	600	-	-	V	Vgs=0V,Id=250µA
ldss	Drain-to-Source Leakage Current			10.0	μA	VDS=600V,VGS=0V
lgss	Gate-to-Source Forward Leakage			100	n A	VGS=+30V VDS=0V
	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		3.7	4.2	Ω	Vgs=10V,Id=1A
$V_{GS(TH)}$	Gate Threshold Voltage	3.0		4.0	V	Vgs=Vds,Id=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time	-	7.8			VDS=250V
trise	Rise Time	-	33		nS	ID=2.0A RG=25Ω (Note:3,4)
td(OFF)	Turn-OFF Delay Time	-	23			
tfall	Fall Time		59			

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		310		pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance		39			
Crss	Reverse Transfer Capacitance		6.1			
Qg	Total Gate Charge		8		nC	VDS=480V ID=2.0A VGS=10V (Note:3,4)
Qgs	Gate-to-Source Charge		1.2			
Qgd	Gate-to-Drain("Miller") Charge		5			

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ls	Continuous Source Current			2	Α	Integral pn-diode
Ism	Maximum Pulsed Current			8	Α	in MOSFET
Vsd	Diode Forward Voltage			1.4	V	Is=2.0A,Vgs=0V
trr	Reverse Recovery Time		80		nS	Vgs=0V
Qrr	Reverse Recovery Charge		1.8		μC	Is=2.0A,di/dt=100A/µs

Notes:

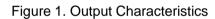
*1.TJ=±25℃ to +150℃.

*2.Repetitive rating; pulse width limited by maximum junction temperature.

*3.Pulse width \leq 300µs; duty cycle \leq 1%.

*4.Basically not affected by temperature.

Typical Feature curve (TJ = 25° C, unless otherwise noted)



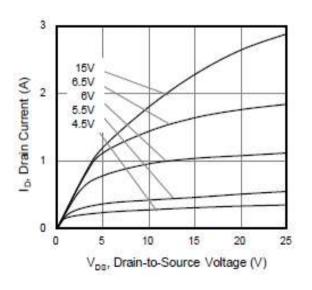


Figure 2. Drain Current vs. Temperature

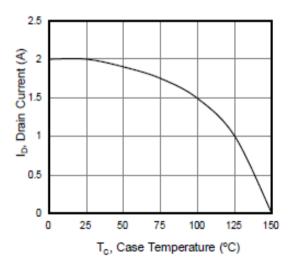




Figure 3. Body Diode Forward Voltage

Figure 4. Power Dissipation vs. Temperature

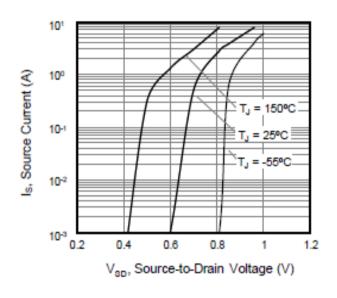
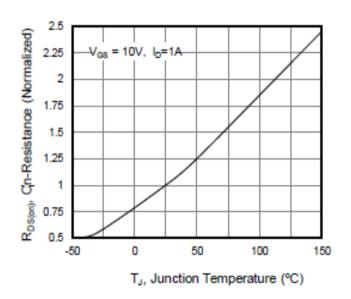


Figure 5. On-Resistance vs. Temperature





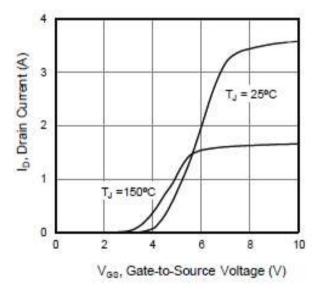
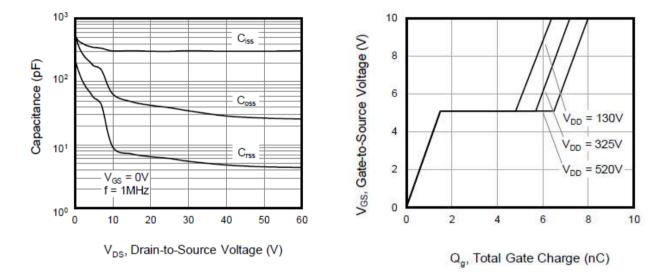




Figure7. Capacitance

Figure8. Gate Charge



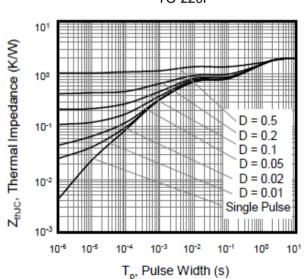
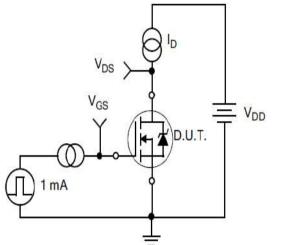


Figure 9. Transient Thermal Impedance TO-220F



Test Circuits and Waveforms



Vgs(TH)

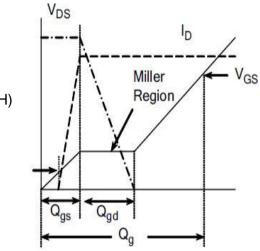
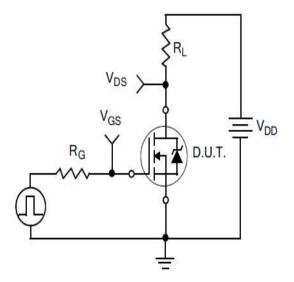


Figure10. Gate Charge Test Circuit

Figure11. Gate Charge Waveform



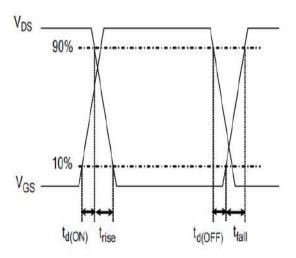


Figure12. Resistive Switching Test Circuit

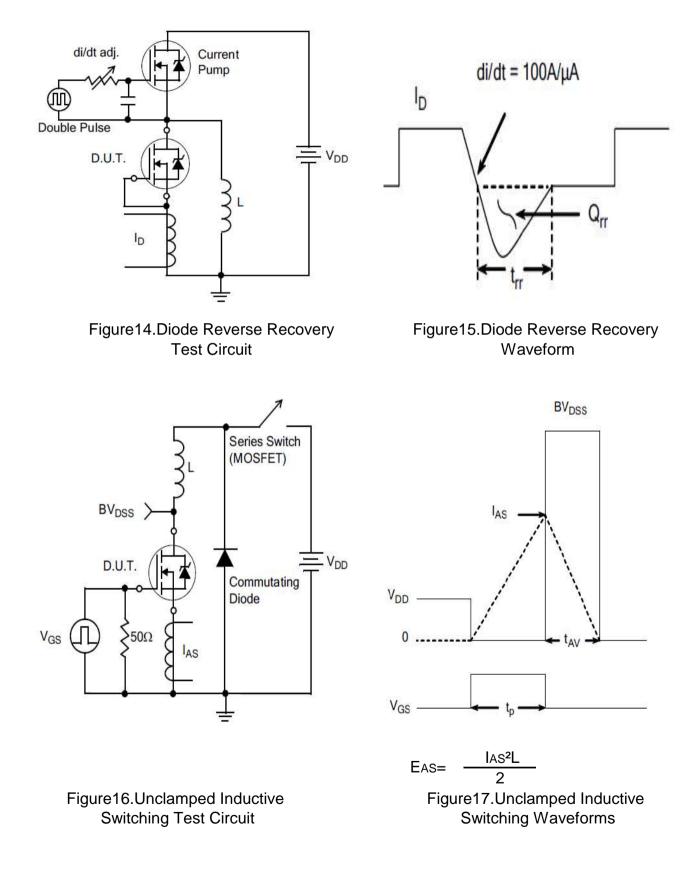
Figure13. Resistive Switching Waveforms

http://www.reasunos.com



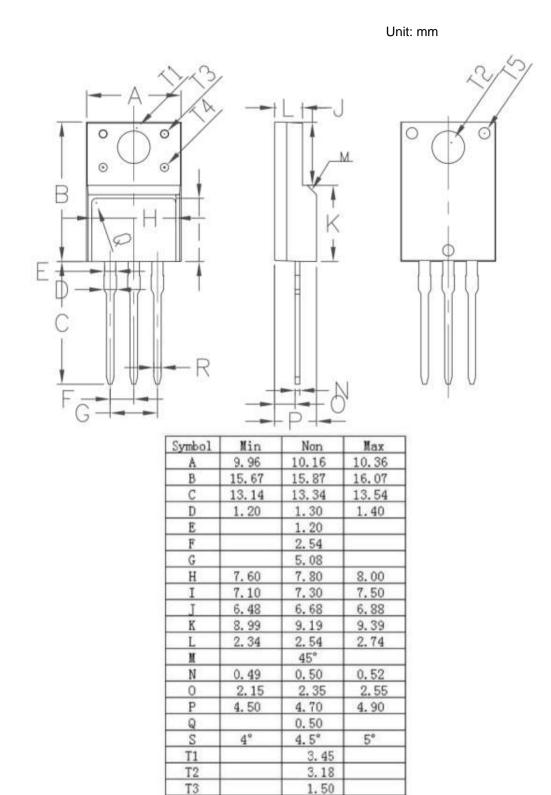
RS2N60F

Test Circuits and Waveforms





Package outline drawing



0.77

T4 T5

R

1.20

1.50

0.8

0.83



Disclaimers:

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information in current and complete. All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components. To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights,nor the rights of others. Reproduction of information in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

1.Life support devices or systems are devices or systems which:

a.are intended for surgical implant into the human body,

b.support or sustain life,

c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.