

RS20N50W

N Channel MOSFET

Applications:

- Adapter & Charger
- •DC-AC inverter Power
- •AC-DC Switching Power Supply
- •LED driving power

Features:

- Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- RoHS Compliant



Lead Free Package and Finish

	ID	RDS(ON)(Typ.)	Vdss
	20A	0.23Ω	500V
ng	G D S TO	1.Gate o	2.Drain

Ordering Information

Part Number	Package	Marking
RS20N50W	TO-247	RS20N50W

Absolute Maximun Ratings Tc=25°C unless otherwise specified

Symbol	Parameter	RS20N50W	Units
VDSS	Drain-to-Source Voltage (Note*1)	500	V
ID	Continuous Drain Current	20.0	
ID@ 100 ℃	Continuous Drain Current	12.6	А
ldм	Pulsed Drain Current (Note*2)	80	
PD	Power Dissipation	230	W
PD	Derating Factor above 25° C	1.85	W/°C
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH VDD=50V RG=25Ω TJ=25℃	1200	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	°C
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS20N50W	Units	Test Conditions
RθJC	Junction-to-Case	0.54		Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.



OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	500			V	Vgs=0V,Id=250µA
ldss	Drain-to-Source Leakage Current			1.0	μA	VDS=500V,VGS=0V
lgss	Gate-to-Source Forward Leakage			100		Vgs=+30V, Vds=0V
IGSS	Gate-to-Source Reverse Leakage			-100	μA	VGS=-30V ,VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter		Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		0.23	0.28	Ω	Vgs=10V,Id=10A
Vgs(TH)	Gate Threshold Voltage	2.0		4.0	V	Vgs=Vds,Id=250µA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		33			
trise	Rise Time		75		nS	VDS=250V ID=20A
td(OFF)	Turn-OFF Delay Time		91		115	$R_{G}=20\Lambda$
tfall	Fall Time		83			

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		1920			Vgs=0V
Coss	Output Capacitance		290		pF	VDS=25V
Crss	Reverse Transfer Capacitance		18			f=1.0MHz
Qg	Total Gate Charge		56			VDS=400V
Qgs	Gate-to-Source Charge		13		nC	ID=20A
Qgd	Gate-to-Drain("Miller") Charge		20			VGS=10V



Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ls	Continuous Source Current			20	Α	Integral pn-diode
lsм	Maximum Pulsed Current			80	А	in MOSFET
Vsd	Diode Forward Voltage			1.2	V	Is=20A,Vgs=0V
trr	Reverse Recovery Time		536		nS	Vgs=0V
Qrr	Reverse Recovery Charge		5.6		μC	Is=20A,di/dt=100A/µs

Notes:

*1.Repetitive rating; pulse width limited by maximum junction temperature.

Typical Feature curve

Figure1 Typical Output Characteristics

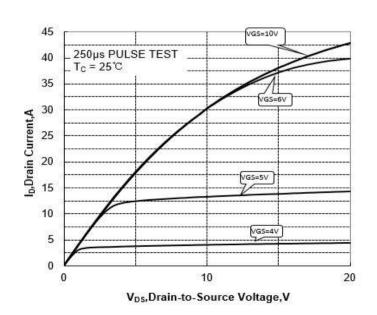
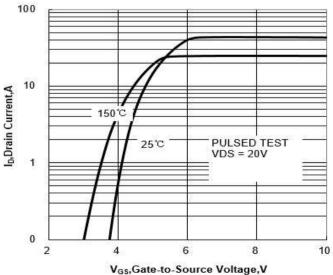


Figure2 Typical Transfer Characteristics



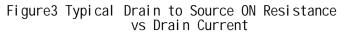
Copyright Reasunos

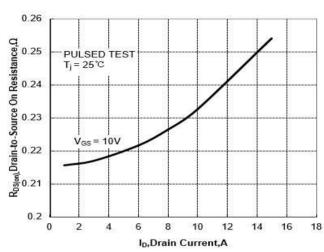
http://www.reasunos.com

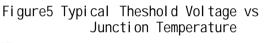
REV:A0 JAN.2022



RS20N50W







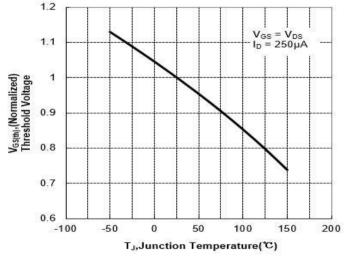
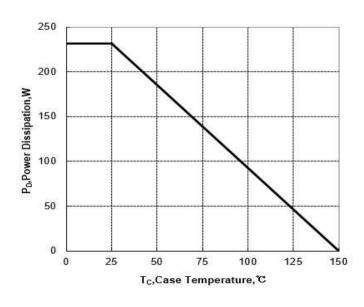


Figure7 Power Dissipation



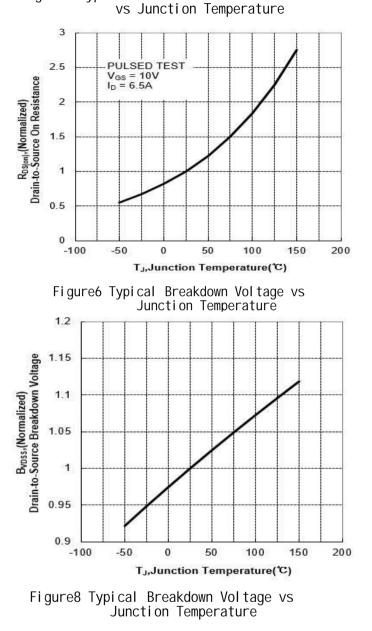
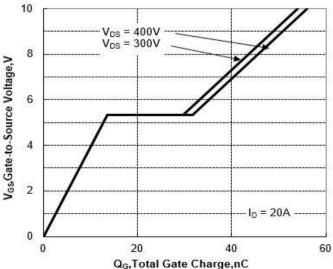


Figure4 Typical Drian to Source on Resistance



REV:A0 JAN.2022



Figure9 Typical Theshold Voltage vs Junction Temperature

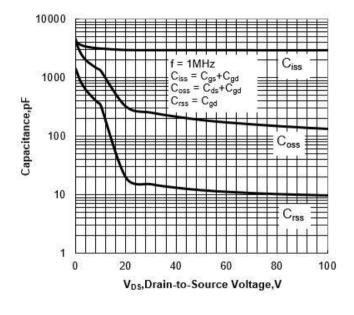


Figure11 Max Thermal Impendance

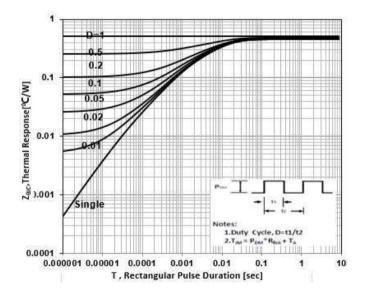
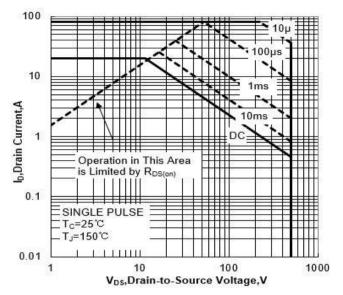
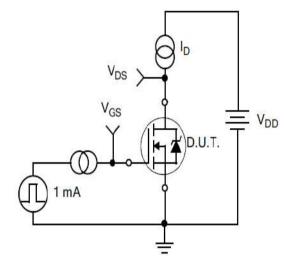


Figure10 Safe Operating Area





Test Circuits and Waveforms



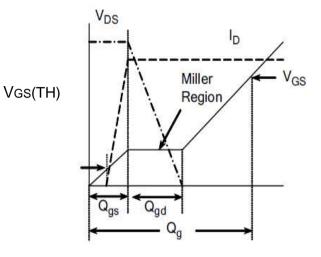


Figure12. Gate Charge Test Circuit

Figure13. Gate Charge Waveform

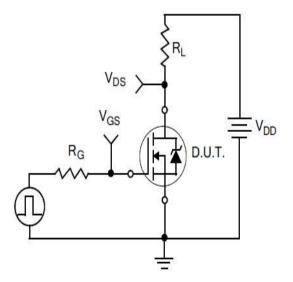


Figure14. Resistive Switching Test Circuit

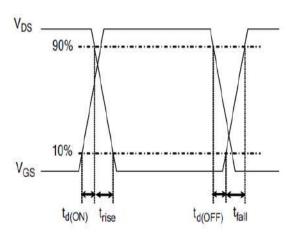


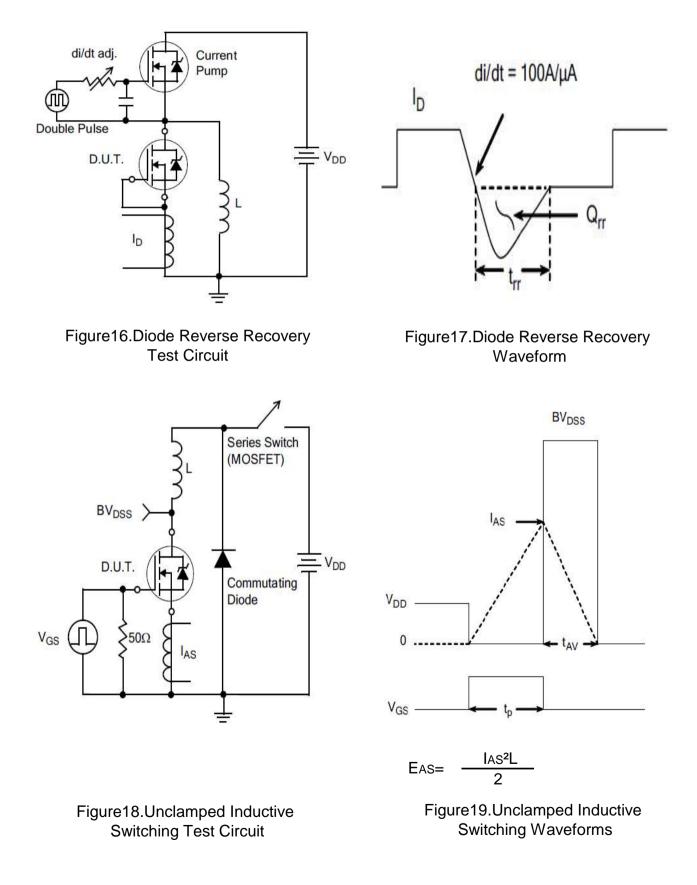
Figure15. Resistive Switching Waveforms

http://www.reasunos.com



RS20N50W

Test Circuits and Waveforms

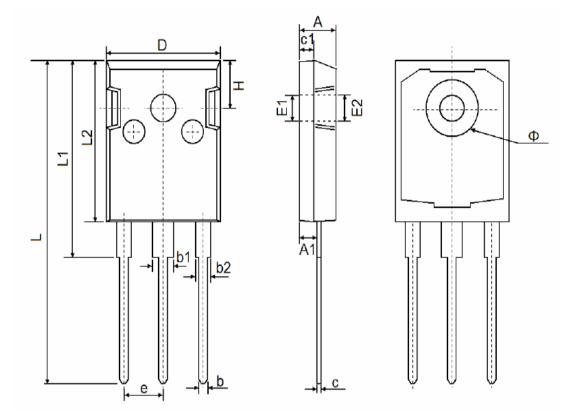




Package outline drawing

Unit:mm

RS20N50W



TO-247

Cumb al	Dimensions	In Millimeters	Dimension	s In Inches	
Symbol	Min.	Max.	Min.	Max.	
А	4.850	5.150	0.191	0.200	
A1	2.200	2.600	0.087	0.102	
b	1.000	1.400	0.039	0.055	
b1	2.800	3.200	0.110	0.126	
b2	1.800	2.200	0.071	0.087	
с	0.500	0.700	0.020	0.028	
c1	1.900	2.100	0.075	0.083	
D	15.450	15.750	0.608	0.620	
E1	3.500 REF		0.138	REF	
E2	3.600 REF		0.142	REF	
L	40.900	41.300	1.610	1.626	
L1	24.800	25.100	0.976	0.988	
L2	20.300	20.600	0.799	0.811	
Φ	7.100	7.300	0.280	0.287	
е	5.450) TYP	0.215	TYP	
Н	5.980) REF	0.235 REF		

Copyright Reasunos

REV:A0 JAN.2022



Disclaimers:

Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability,function or design and to discontinue any product or service without notice .Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale.Testing,reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement,testing of all parameters of each product is not necessarily performed.

Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk,customers must provide adequate design and operating safeguards.

Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights,nor the rights of others.Reproduction of information in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration.Reproduction of this information with any alteration is an unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

Life Support Policy:

Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Reasunos Semiconductor Technology CO.,LTD.

As used herein:

1.Life support devices or systems are devices or systems which:

a.are intended for surgical implant into the human body,

b.support or sustain life,

c.whose failuer to when properly used in accordance with instructions for used provided in the laeling,can be reasonably expected to result in significant injury to the user.

2.A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.