

## **N Channel MOSFET**

## Applications:

- Adapter & Charger
- SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

#### Features:

- •Low On Resistance
- Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

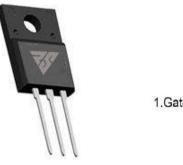
# **Ordering Information**

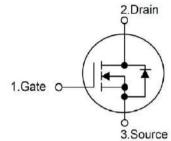
Part Number	Package	Marking
RS12N65F	TO-220F	RS12N65F



Lead Free Package and Finish

lo	RDS(ON)(Typ.)	VDSS
12A	0.6Ω	650V





Not to Scale

# Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS12N65F	Units
VDSS	Drain-to-Source Voltage (Note*1)	650	V
lD	Continuous Drain Current	12.0	
ID@ 100 ℃	Continuous Drain Current	7.2	Α
ldм	Pulsed Drain Current (Note*2)	48.0	
DD	Power Dissipation	70	W
PD	Derating Factor above 25℃	0.56	W/°C
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH VDD=150V RG=25Ω TJ=25℃	810	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	300 260	$^{\circ}$
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage	-55 to 150	
10 4114 1010	Temperature Range	30 10 100	

<sup>\*</sup>Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

#### **Thermal Resistance**

Symbol	Parameter	RS12N65F	Units	Test Conditions
Rejc	Junction-to-Case	1.92	.c\M	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
RөJA	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

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## OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650			٧	Vgs=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1.0	μΑ	VDS=650V,VGS=0V
loos	Gate-to-Source Forward Leakage			100	n 1	Vgs=+30V Vps=0V
Igss	Gate-to-Source Reverse Leakage	-	1	-100	nA	Vgs=-30V Vps=0V

# ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		0.6	0.75	Ω	Vgs=10V,ID=6A
Vgs(TH)	Gate Threshold Voltage	2.0		4.0	V	Vgs=Vps,Ip=250µA
gfs	Forward Trans conductance			12	S	VDS=15V,ID=6A

# Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		28			Vps=325V
trise	Rise Time		29		nS	ID=12A
td(OFF)	Turn-OFF Delay Time		86		113	Rg=25Ω
tfall	Fall Time		31			(Note:3,4)

# Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		2023			Vgs=0V
Coss	Output Capacitance		159		pF	VDS=25V
Crss	Reverse Transfer Capacitance		8			f=1.0MHz
Qg	Total Gate Charge		39			Vps=520V
Qgs	Gate-to-Source Charge		10		nC	I <sub>D</sub> =12A VGS=10V
Qgd	Gate-to-Drain("Miller") Charge		15			(Note:3,4)

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#### **Source-Drain Diode Characteristics**

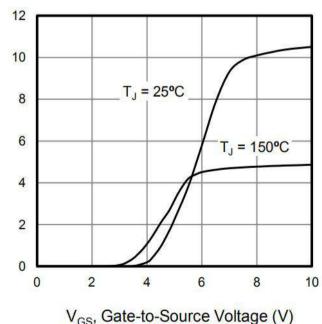
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current	-	-	12	Α	Integral pn-diode
Ism	Maximum Pulsed Current	-	-	48	Α	in MOSFET
VsD	Diode Forward Voltage	-	-	1	V	Is=12A,Vgs=0V
trr	Reverse Recovery Time		521		nS	Vgs=0V
Qrr	Reverse Recovery Charge		4.1		μC	Is=10A,di/dt=100A/μs

#### Notes:

## **Typical Feature curve**

**Figure 1. Typical Output Characteristics** 16 20V 14 10V 87 ID, Drain Current (A) 12 I<sub>D</sub>, Drain Current (A) **7V** 6V 10 **5V** 8 4 2 0 8 10 12 14 16 18 20 0 V<sub>DS</sub>, Drain-to-Source Voltage (V)

**Figure 2. Typical Transfer Characteristics** 



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<sup>\*1.</sup>TJ=±25℃ to +150℃.

<sup>\*2.</sup>Repetitive rating; pulse width limited by maximum junction temperature.

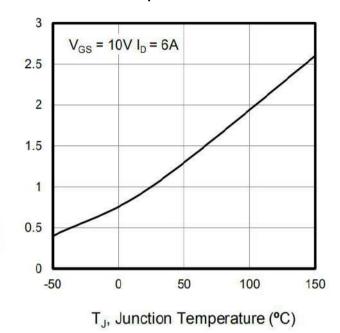
<sup>\*3.</sup> Pulse width  $\leq$  300 µs; duty cycle  $\leq$  1%.

<sup>\*4.</sup>Basically not affected by temperature.



R<sub>DS(on)</sub>, On-Resistance (Normalized)

Figuer3.Typical ON Resistance vs
Temperature



Figuer4.Typical Body Diode Transfer Characteristics

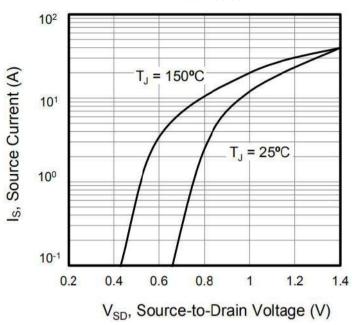


Figure5.Typical Drain current vs.
Temperature

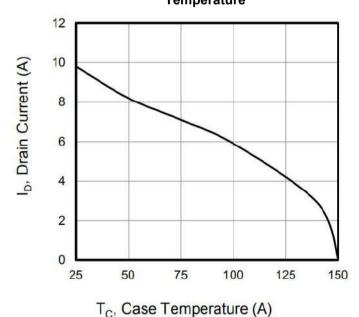
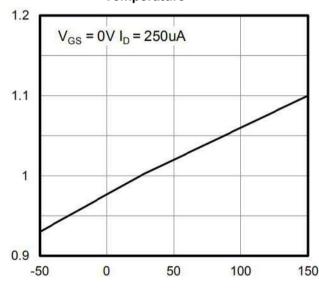


Figure 6. BVDSS Variation vs. Temperature



T<sub>J</sub>, Junction Temperature (°C)

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BV<sub>DSS</sub> (Normalized)



Figure 7. Capacitance vs. Drain to Source Voltage

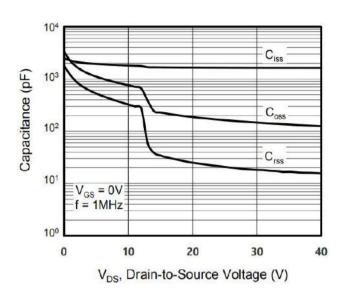


Figure8. Gate Charge

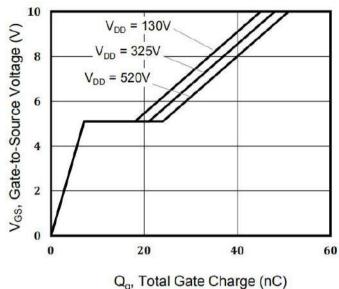
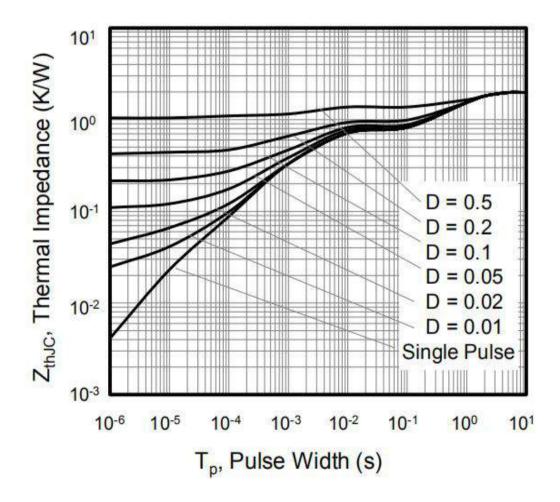


Figure9. Transient Thermal Impedance



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# **Test Circuits and Waveforms**

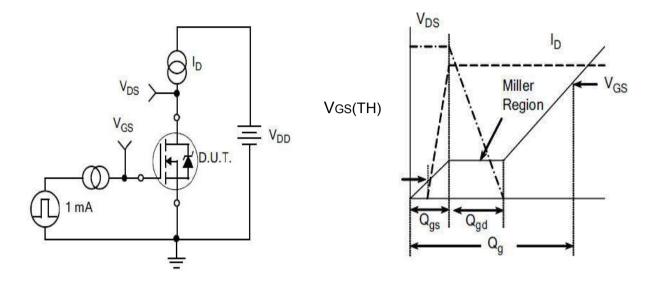


Figure11.
Gate Charge Test Circuit

Figure 12.
Gate Charge Waveform

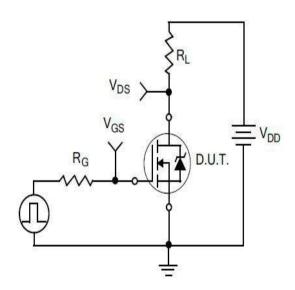


Figure 13.
Resistive Switching Test Circuit

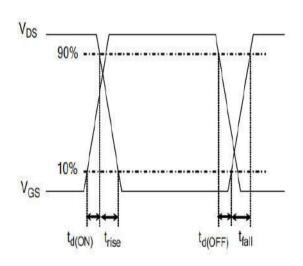


Figure 14.
Resistive Switching Waveforms

## **Test Circuits and Waveforms**

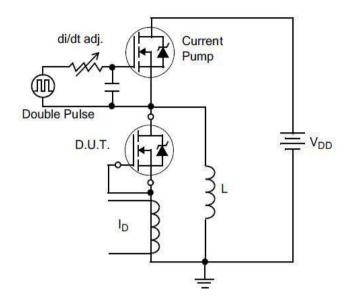


Figure 15. Diode Reverse Recovery
Test Circuit

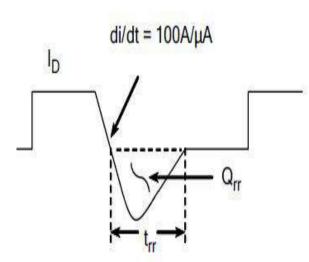


Figure 16. Diode Reverse Recovery Waveform

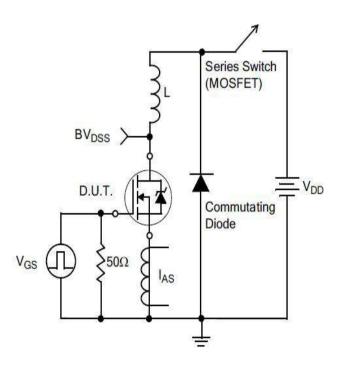
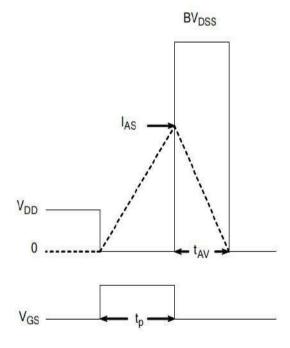


Figure 17. Unclamped Inductive Switching Test Circuit



Eas= 
$$\frac{\text{Ias}^2\text{L}}{2}$$

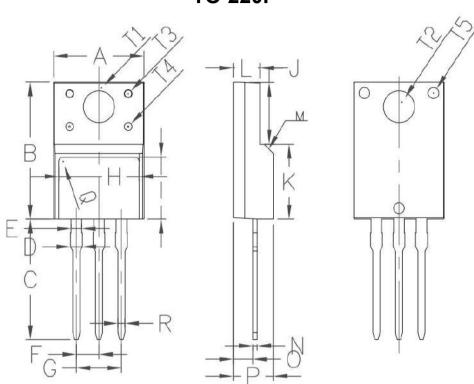
Figure 18. Unclamped Inductive Switching Waveforms



# Package outline drawing







Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
С	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
Н	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8. 99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
0	2.15	2.35	2.55
P	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3.45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83

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