2.Drain

3.Source



N Channel MOSFET

Applications:

- Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

Features:

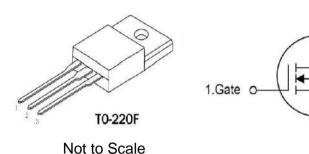
- Low On Resistance
- Low Gate Charge
- •Improved dv/dt capability
- •RoHS Compliant

Ordering Information

Part Number	Package	Marking
RS10N80F	TO-220F	RS10N80F

Lead Free Package and Finish

ΙD	Rds(ON)(Typ.)	VDSS
10A	1.0Ω	800V



Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS10N80F	Units
VDSS	Drain-to-Source Voltage	800	V
ID	Continuous Drain Current	10	А
IDМ	Pulsed Drain Current (Note*1)	40	A
PD	Power Dissipation	25	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy (Note*2)	405	mJ
IAS	Avalanche Current (Note*1)	9	А
EAR	Repetitive Avalanche Energy (Note*1)	243	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	${\mathbb C}$
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

^{*}Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS10N80F	Units	Test Conditions
Rejc	Junction-to-Case	5	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150°C.
Reja	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

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OFF Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	800			V	VGS=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1	μΑ	VDS=800V,VGS=0V
IGSS	Gate-to-Source Forward Leakage			100	nΛ	VGS=+30V VDS=0V
1000	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (Note*3)	1	1.0	1.2	Ω	VGS=10V,ID=5A
VGS(th)	Gate Threshold Voltage	3.0		4.0	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		45			
trise	Rise Time		17		nS	VDS=400V ID=10A
td(OFF)	Turn-OFF Delay Time		355		113	RG=25Ω
tfall	Fall Time		475			

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		1519			VGS=0V
Coss	Output Capacitance		162		pF	VDS=25V
Crss	Reverse Transfer Capacitance		34			f=1.0MHz
Qg	Total Gate Charge		57			VDS=640V
Qgs	Gate-to-Source Charge		24		nC	ID=10A
Qgd	Gate-to-Drain("Miller") Charge		7.5			VGS=10V

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Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current		-	10	Α	Integral pn-diode
ISM	Maximum Pulsed Current			40	Α	in MOSFET
VSD	Diode Forward Voltage			1.4	V	IS=5A,VGS=0V
trr	Reverse Recovery Time		562		ns	VGS=0V
Qrr	Reverse Recovery Charge		4.4		μC	IS=10A,di/dt=100A/μs

Notes:

Typical Feature curve TJ = 25°C, unless otherwise noted

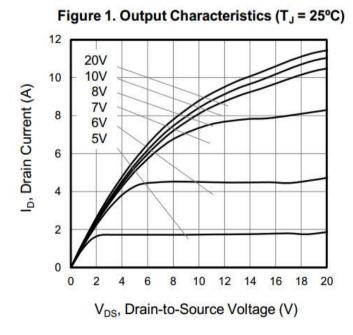
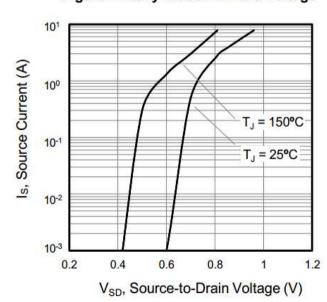


Figure 2. Body Diode Forward Voltage



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^{*1.}Repetitive rating; pulse width limited by maximum junction temperature.

^{*2.}L=10mH, VDD = 50V, RG = 25 Ω , Starting TJ = 25 $^{\circ}$ C

^{*3.}Pulse Test: Pulse width \leqslant 300µs, Duty Cycle \leqslant 1%



Io, Drain Current (A)

Figure 3. Drain Current vs. Temperature

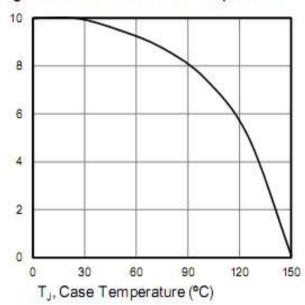


Figure 4. BV_{DSS} Variation vs. Temperature

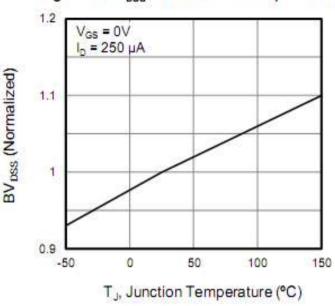


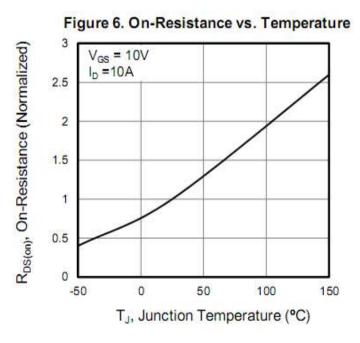
Figure 5. Transfer Characteristics

T_J = 25°C

T_J = 150°C

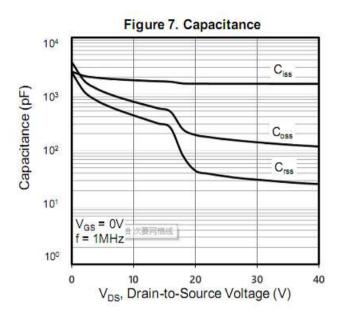
T_J = 150°C

V_{GS}, Gate-to-Source Voltage (V)



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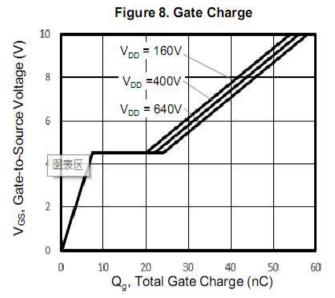
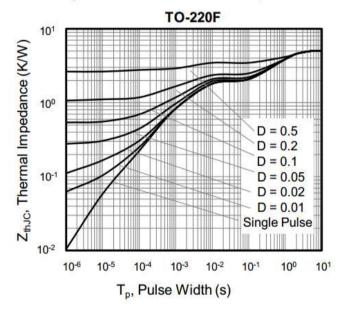


Figure 9. Transient Thermal Impedance





Test Circuits and Waveforms

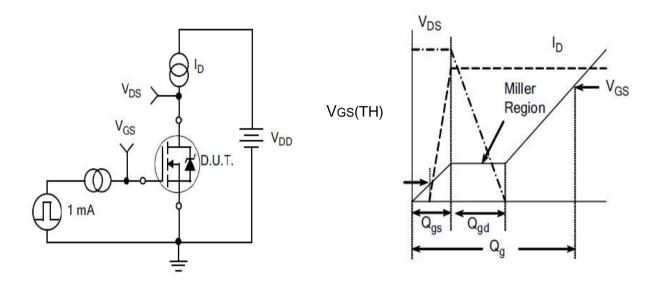


Figure A.
Gate Charge Test Circuit

Figure B.
Gate Charge Waveform

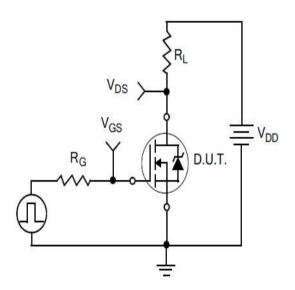


Figure C.
Resistive Switching Test Circuit

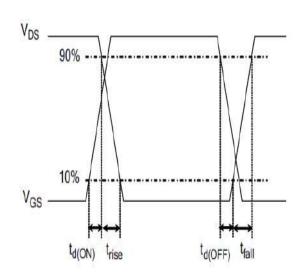


Figure D.
Resistive Switching Waveforms



Test Circuits and Waveforms

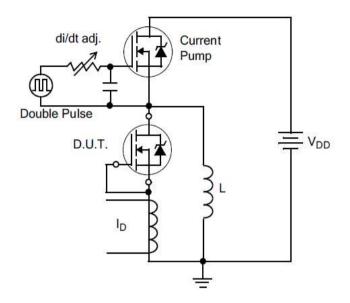


Figure E.Diode Reverse Recovery
Test Circuit

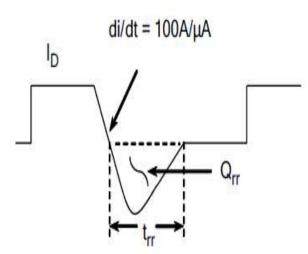


Figure F.Diode Reverse Recovery Waveform

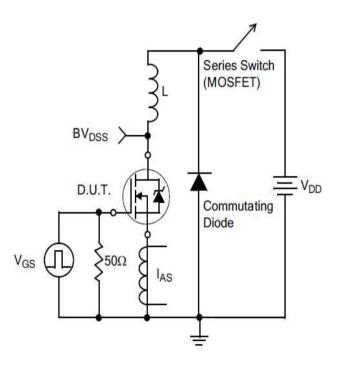
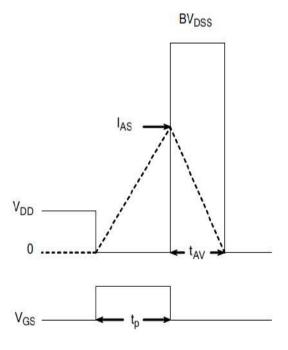


Figure G.Unclamped Inductive Switching Test Circuit



$$EAS = \frac{IAS^2L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

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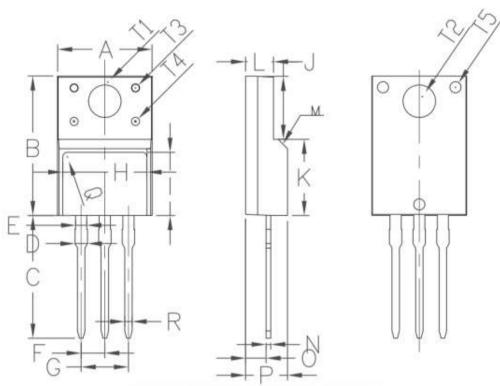
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Package outline drawing





Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
C	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
H	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8.99	9.19	9.39
L	2.34 2.54		
M		45°	
N	0.49	0.50	0.52
0	2.15	2.35	2.55
P	4.50	4.70	4.90
Q		0.50	37.000
S	4°	4.5°	5°
T1		3. 45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83

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