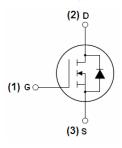


N-Channel Enhancement Mode Power MOSFET

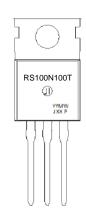


Description

The RS100N100T uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.



Schematic diagram



Marking and pin assignment

General Features

- $V_{DS} = 100V, I_D = 100A$ $R_{DS(ON)} < 13mΩ @ V_{GS} = 10V$ (Typ:9.9mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-220 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
RS100N100T	RS100N100T	TO-220	-	-	-

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Symbol	Parameter	Limit	Unit
V _{DS}	Drain-Source Voltage	100	V
V _G s	Gate-Source Voltage	±20	V
I _D	Drain Current-Continuous	100	Α
I _D (100℃)	Drain Current-Continuous(TC=100℃)	80	Α
I _{DM}	Pulsed Drain Current	380	Α
P _D	Maximum Power Dissipation	200	W
	Derating factor	1.33	W/℃
E _{AS}	Single pulse avalanche energy (Note 5)	800	mJ
T_{J}, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^{\circ}$



Thermal Characteristic

$R_{ heta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	0.75	°C/W
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Electrical Characteristics (T_C=25 °C unless otherwise noted)

Sy	mbol	Parameter	Condition	Min	Тур	Max	Unit
Off Characteristics				•			
BV _{DSS}	Drain-Source Break	down Voltage	V _{GS} =0V I _D =250μA	100	110	-	V
I _{DSS}	Zero Gate Voltage I	Orain Current	V _{DS} =100V,V _{GS} =0V	-	-	1	μΑ
I _{GSS}	Gate-Body Leaka	ge Current	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics	(Note 3)						
V _{GS(th)}	Gate Threshold	l Voltage	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
R _{DS(ON)}	Drain-Source On-Sta	te Resistance	V _{GS} =10V, I _D =40A -		9.9	13	mΩ
g _{FS}	Forward Transco	nductance	V _{DS} =50V,I _D =40A	100	-	-	S
Dynamic Character	istics (Note4)						
C _{lss}	Input Capac	itance	\/ F0\/\/ 0\/	-	4800	-	PF
C _{oss}	Output Capac	citance	V_{DS} =50V, V_{GS} =0V, F=1.0MHz	-	340	-	PF
C _{rss}	Reverse Transfer (Capacitance	F=1.UIVITZ	-	150	-	PF
Switching Characte	eristics (Note 4)			•			
t _{d(on)}	Turn-on Dela	y Time		-	15	-	nS
t _r	Turn-on Rise	Time	V _{DD} =50V,I _D =40A	-	50	-	nS
t _{d(off)}	Turn-Off Dela	y Time	V_{GS} =10V, R_{GEN} =2.5 Ω	-	40	-	nS
t _f	Turn-Off Fall	Time		-	55	-	nS
Q _g	Total Gate C	harge	V _{DS} =80V,I _D =40A,	-	85	-	nC
Q _{gs}	Gate-Source	Charge	$V_{DS}=80V,I_{D}=40A,$ $V_{GS}=10V$	-	18	-	nC
Q_{gd}	Gate-Drain C	harge	V _{GS} =10V	-	28	-	nC
Drain-Source Diode	Characteristics						
V _{SD}	Diode Forward Vo	oltage (Note 3)	V _{GS} =0V,I _S =40A	-	-	1.2	V
Is	Diode Forward Cu		-	-	-	57	Α
t _{rr}	Reverse Recove	ery Time	TJ = 25°C, IF = 40A	-	38	80	nS
Qrr	Reverse Recover	ry Charge	di/dt = 100A/μs(Note3)	-	53	100	nC
t _{on}	Forward Turn-C	On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+			y LS+LD)	

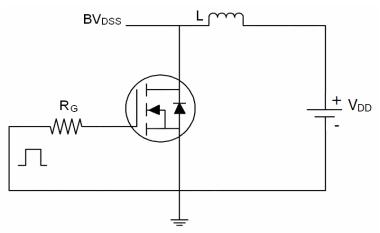
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- 5. EAS condition:Tj=25 $^{\circ}$ C,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25 Ω

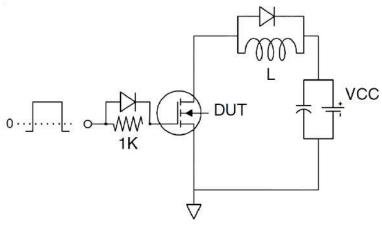


Test Circuit

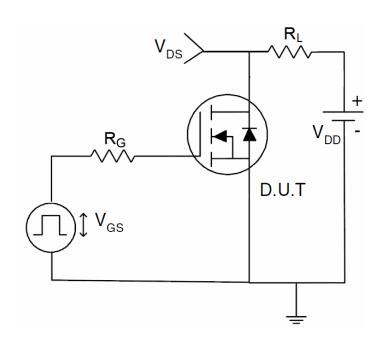
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

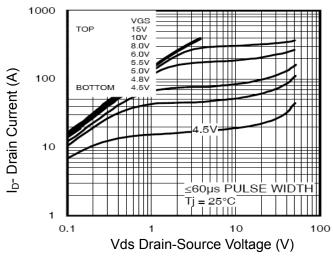


Figure 1 Output Characteristics

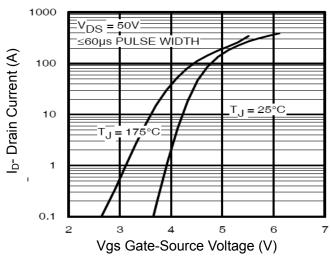


Figure 2 Transfer Characteristics

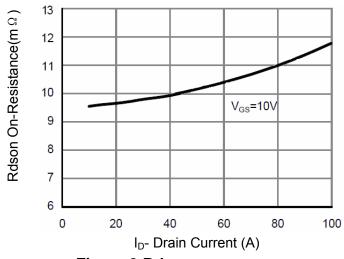


Figure 3 Rdson- Drain Current

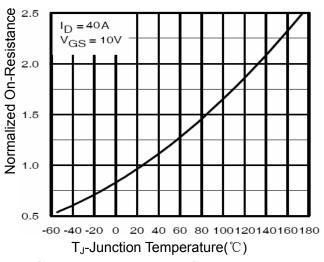


Figure 4 Rdson-JunctionTemperature

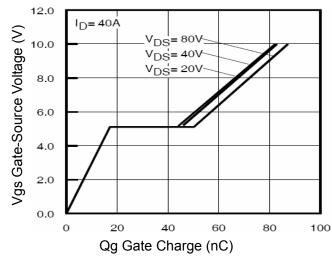


Figure 5 Gate Charge

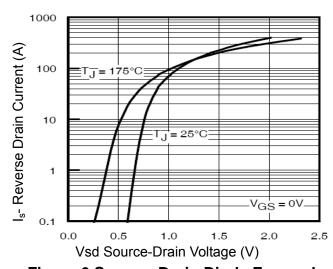
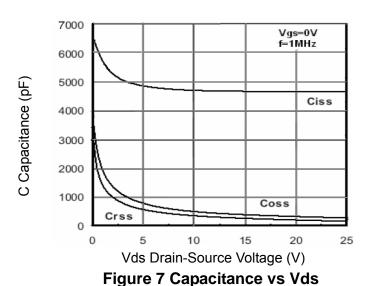


Figure 6 Source- Drain Diode Forward



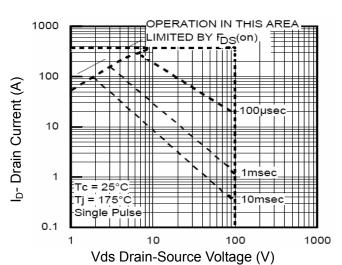


Figure 8 Safe Operation Area

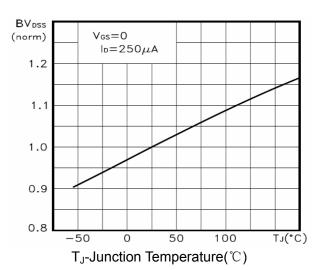


Figure 9 BV_{DSS} vs Junction Temperature

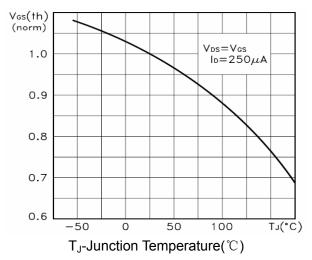


Figure 10 V_{GS(th)} vs Junction Temperature

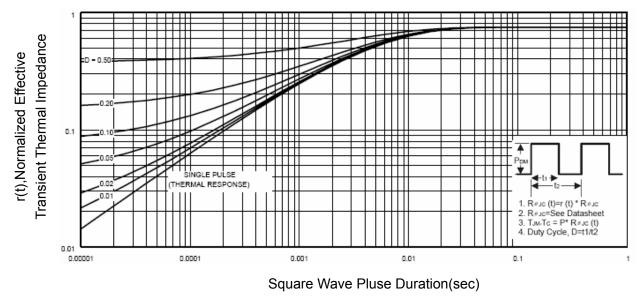
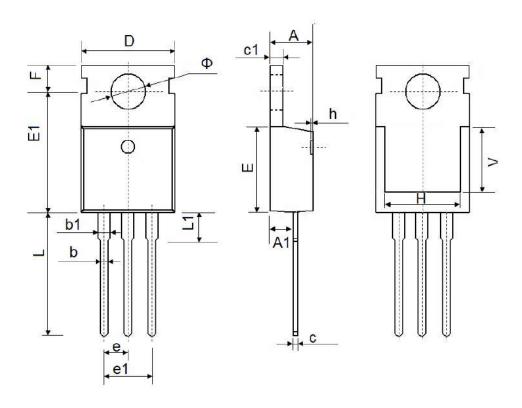


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Compleal	Dimensions	In Millimeters	Dimensions In Inches			
Symbol	Min.	Max.	Min.	Max.		
A	4.400	4.600	0.173	0.181		
A1	2.250	2.550	0.089	0.100		
b	0.710	0.910	0.028	0.036		
b1	1.170	1.370	0.046	0.054		
С	0.330	0.650	0.013	0.026		
c1	1.200	1.400	0.047	0.055		
D	9.910	10.250	0.390	0.404		
E	8.9500	9.750	0.352	0.384		
E1	12.650	12.950	0.498	0.510		
е	2.54	10 TYP. 0.1		00 TYP.		
e1	4.980	5.180	0.196	0.204		
F	2.650	2.950	0.104	0.116		
Н	7.900	8.100	0.311	0.319		
h	0.000	0.300	0.000	0.012		
L	12.900	13.400	0.508	0.528		
L1	2.850	3.250	0.112	0.128		
V	7.50	7.500 REF.		0.295 REF.		
Ф	3.400	3.800	0.134	0.150		



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